FS45/FS65 FAQ

Frequently Asked Questions V2.0

MAY 2021

SECURE CONNECTIONS
FOR A SMARTER WORLD

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CATALOG OVERVIEW

WHAT APPLICATION FS45/FS65 CAN BE USED ?

Drive Train Electrification

BMS, Hybrid EV and HEV, Inverter, DCDC, Alterno Starter

Drive Train - Chassis & Safety

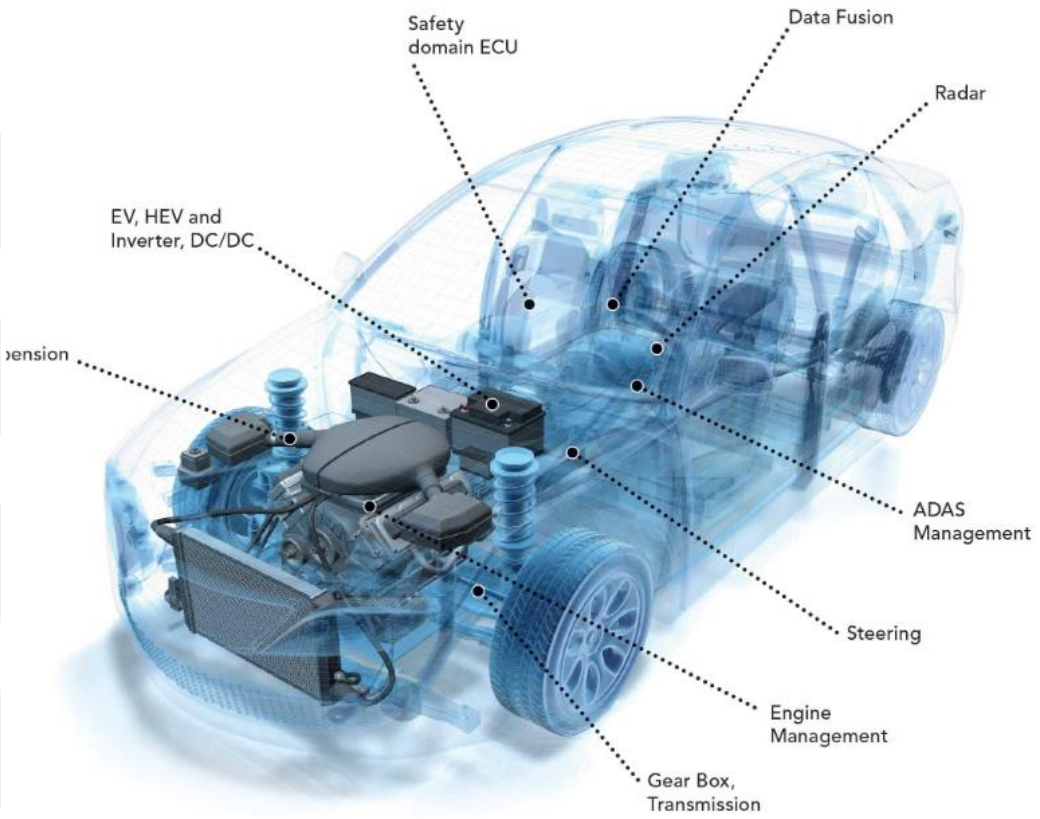
Active Suspension, Steering, Safety Domain Gateway

Power Train

EMS, TCU, Gear Box

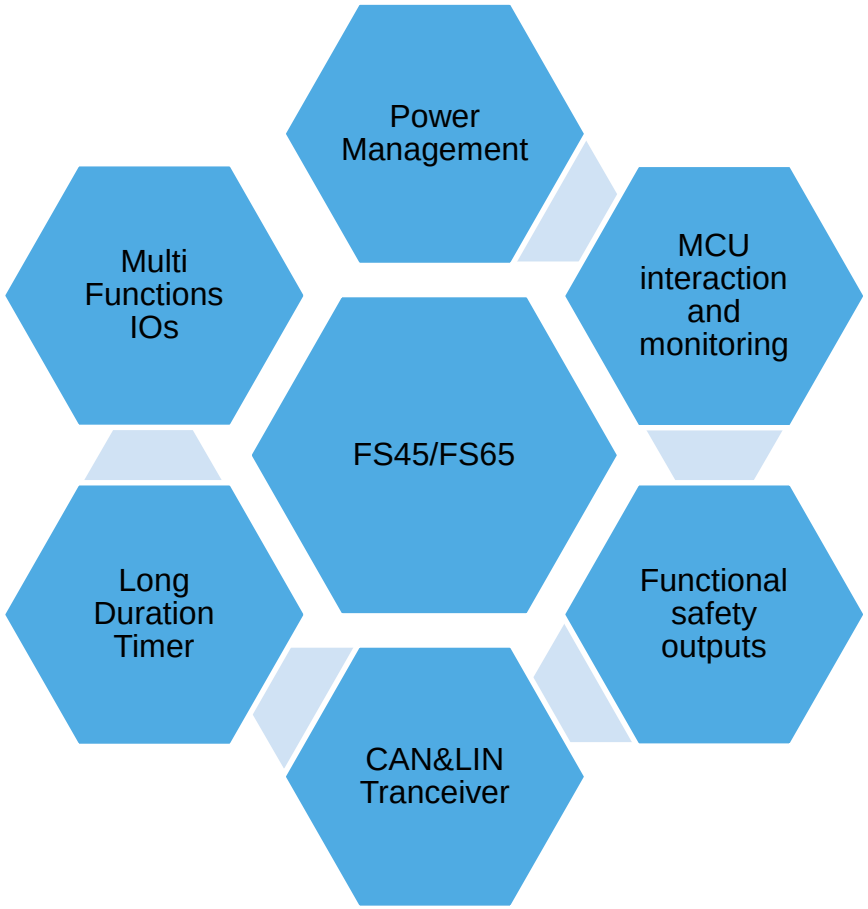
ADAS

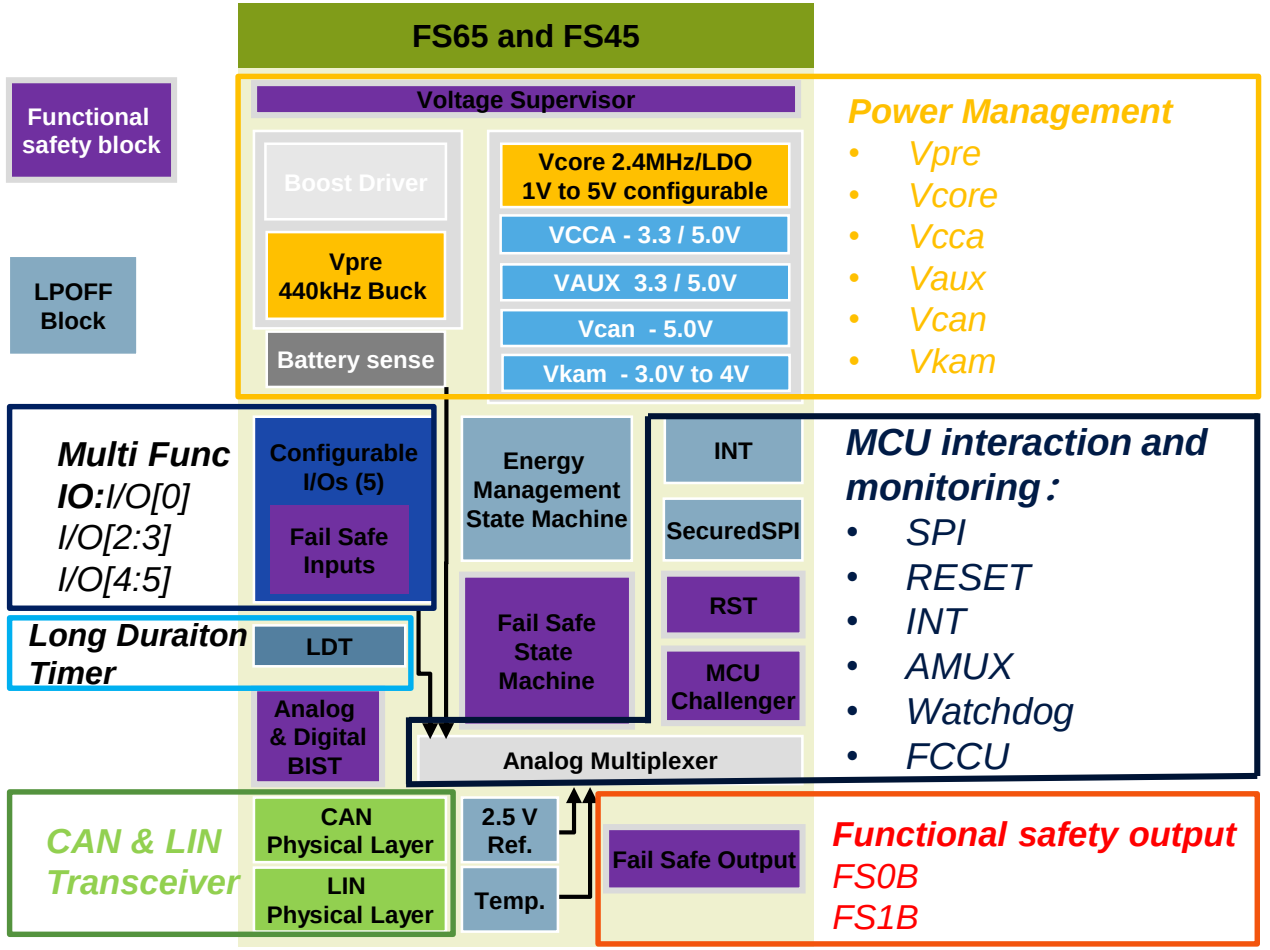
LDW, Radar, Sensor Fusion Safety area



FS4500/FS6500 Application in Automotive

FS45/FS65 OVERVIEW FUNCTION





FS4500/FS6500 Main Function Blocks

HOW TO SELECT FS45/FS65 PART NUMBER ?

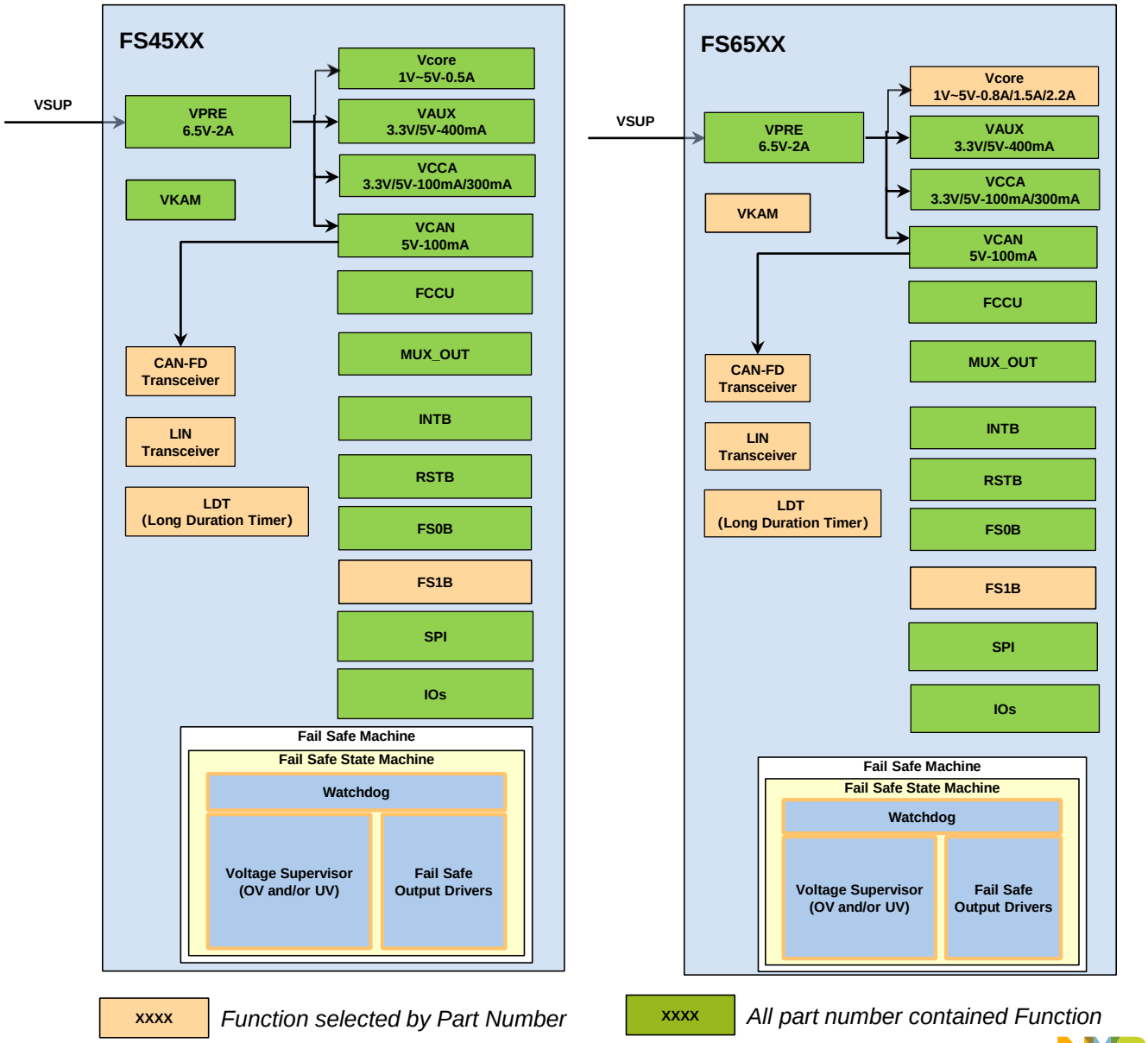
- *FS45XX Vcore is Linear Regulator with 0.5A capability;*
- *FS65XX Vcore is Buck with 0.8A/1.5A/2.2A Selectable;*

FS45xx Part:

***(1) CAN Transceiver**: Part number decide exist or not;*
***(2) LIN Transceiver**: Part number decide exist or not;*
***(3) LDT**: Part number decide exist or not;*
***(4) FS1B**: Part number decide exist or not;*

FS65xx Part:

***(1) Vcore Current Capability**: Part number decide 0.8A/1.5A/2.2A*
***(2) CAN Transceiver:** Part number decide exist or not;*
***(3) LIN Transceiver:** Part number decide exist or not;*
***(4) LDT:** Part number decide exist or not;*
***(5) FS1B:** Part number decide exist or not;*
***(6) VKAM**: Part number decide ON by default or ON by SPI;*



HOW TO SELECT FS45/FS65(ASIL D) PART NUMBER ?

MC 33 FS C 5 x y z AE / R2

QUALIFICATION STATUS:
- **PC** PRE-QUALIFICATION, ENGINEERING SAMPLES
- **MC** FULLY QUALIFIED

TEMPERATURE RANGE:
- **33** T_a = -40°C to 125°C
- **35** T_a = -40°C to 150°C

DEVICE FAMILY DESIGNATOR:
FS : Functional Safety

Family Segmentation
C=6 series : Vcore DCDC
C=4 series : Vcore Linear

SBC Generation
5th generation of SBC devices

TAPE AND REEL DESIGNATOR:
R2 TAPE AND REEL

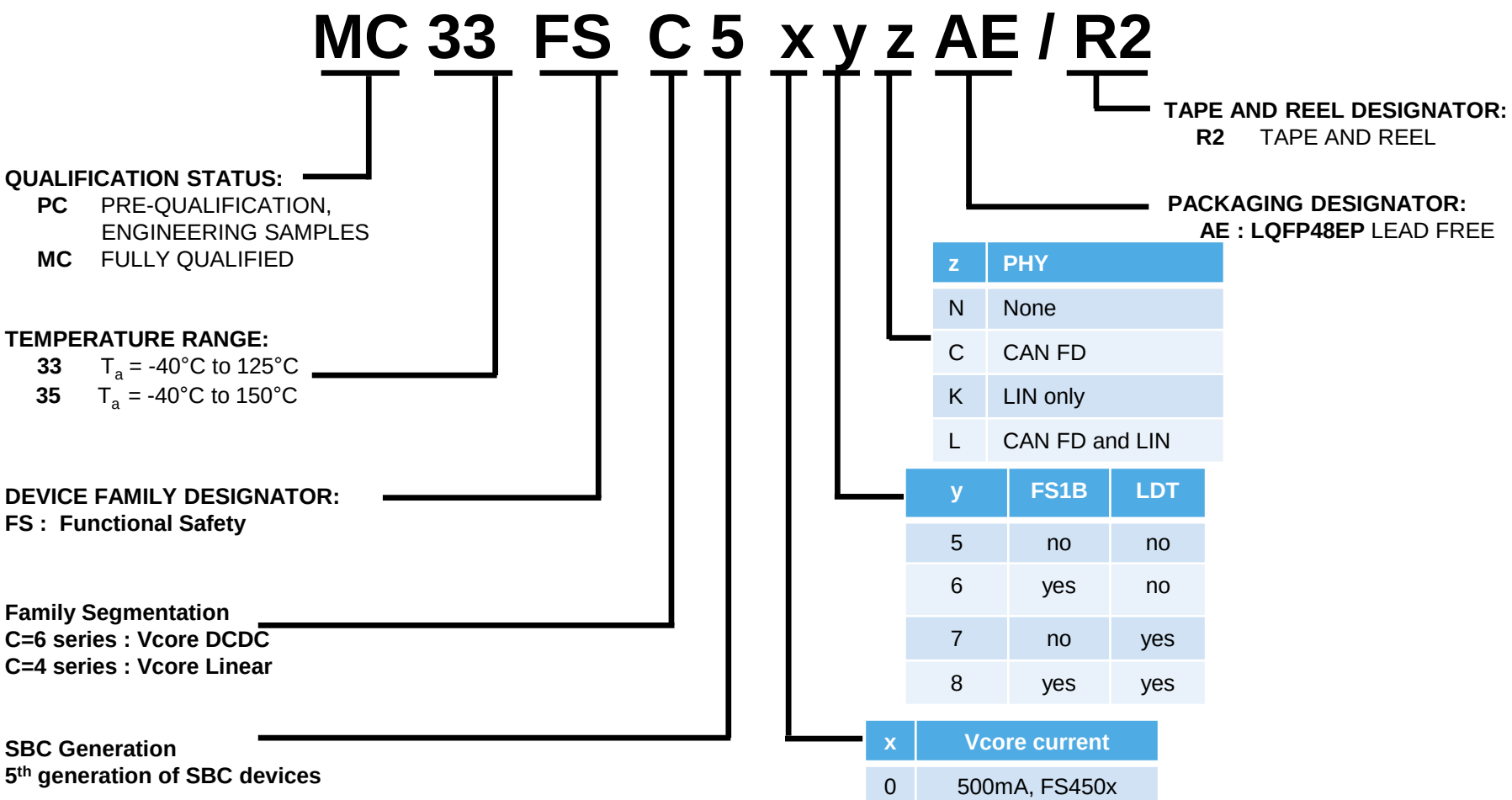
PACKAGING DESIGNATOR:
AE : LQFP48EP LEAD FREE

z	PHY
N	None
C	CAN FD
L	CAN FD and LIN

y	FS1B	LDT	VKAM ON BY DEFAULT
0	no	no	no
1	yes	no	no
2	no	yes	no
3	yes	yes	no
4	no	yes	yes

x	Vcore current
0	500mA, FS450x
0	800mA, FS650x
1	1.5A, FS651x
2	2.2A, FS652x

HOW TO SELECT FS45/FS65(ASIL B) PART NUMBER ?



z	PHY
N	None
C	CAN FD
K	LIN only
L	CAN FD and LIN

y	FS1B	LDT
5	no	no
6	yes	no
7	no	yes
8	yes	yes

x	Vcore current
0	500mA, FS450x
0	800mA, FS650x
1	1.5A, FS651x
2	2.2A, FS652x

FS45/FS65(ASIL D) RECOMMENDED APPLICATION CIRCUIT & SCHEMATIC CHECK-LIST

- *Please refer to* ***Page 133*** *in Datasheet V7.0 for* ***Figure 73. FS6500 simplified application schematic with CAN, FS1B, VKAM, buck/boost VPRE configuration.***
- *Please refer to* ***Page 134*** *in Datasheet V7.0 for* ***Figure 74. FS4500 simplified application schematic with CAN, LIN, IO_5, buck only VPRE configuration.***

Schematic Check List

Name	PIN	I/O	Description	Recommended Connection	Not Used Features
Vsup1/ Vsup2	1/2	I	Device Input pins	• Reverse Protection between battery and Vsup pins, Pi filter inductor selection: L≤2.2uH • Input capacitor should be placed close to Vsup1/2 pins.	N/A
Vsense	3	I	Battery Sense	• Vsense pin connect to battery(prior to reverse protection diode) • 5.1KΩ series resistor/1uF capacitor to ensure AMUX output accuracy and ISO7637 Robust	N/A
Vsup3	4	I	Input pin	• Vsup3 pin connected prior to PI filter • Input capacitor should be placed close to Vsup3 pin.	N/A
LIN/ FS1B	5	I/O	LIN or FS1B	• LIN and FS1B functions are exclusive. When used as FS1B, pull up to VPU_FS • FS1B： 5.1KΩ series resistor used to against ISO 7637-2 • FS1B: 22nF capacitor used to robust against ESD GUN test up to ±8kV, please place this capacitor close to FS1B pin.	Floating
IO_4	10	I/O	Multi Function IO	• When used as Digital input(Wake up capability), external 5.1KΩ resistor & 470nF capacitor for ISO 7637-2 Robust. • Input current within -5mA~5mA;	5.1KΩ resistor pull down to GND
IO5/ VKAM	11	I/O	Multi Function IO	• When used as Digital input(Wake up capability), external 5.1KΩ resistor & 470nF capacitor for ISO 7637-2 Robust. • Input current within -5mA~5mA; • If used as VKAM function, 220nF capacitor is needed. For MC33FS6504LAE MC33FS6514LAE, VKAM is ON by default.	• 5.1KΩ resistor pull down to GND • 220nF capacitor for VKAM ON by default part
IO_0	12	I/O	Multi Function IO	• Wake up pin for DFS mode, usually connect to KL15/wake up sources. external 5.1KΩ resistor & 470nF capacitor for ISO 7637-2 Robust. • Input current within -5mA~5mA;	External pull down to GND (Deep fail-safe should be disabled - SELECT pin connected to VPRE)
FCRBM	13	I	Vcore resistor monitoring	• This pin is used to monitor the middle point of a redundant resistor bridge connected on VCORE	If not used, this pin must be connected directly to FB_CORE

FS45/FS65(ASIL D) RECOMMENDED APPLICATION CIRCUIT & SCHEMATIC CHECK-LIST

Schematic Check List

Name	PIN	I/O	Description	Recommended Connection	Not Used Features
FS0B	14	O	Functional safety output	• 5.1KΩ Pull up to VDDIO • 5.1KΩ series resistor used for ISO 7637-2:2011 Robust. • 22nF capacitor used to robust against ESD GUN test up to ±8kV, place this capacitor close to FS0B pin.	Floating
IO2	18	I	Multi Function IO	• When used as FCCU function, 10KΩ pull down to GND, connect to MCU FCCU_F[0](require output High when MCU is normal and PS=0) • When Cooperate with Aurix MCU SMU, 10KΩ pull down to GND and IO2 connect to SMUFSP Pin; • When used as Digital input for wakeup capability, IO2 voltage cannot exceed 8V;	Open/ 5.1KΩ resistor pull down to GND
IO3	19	I	Multi Function IO	• When used as FCCU function, 5.1KΩ pull up to VDDIO, connect to MCU FCCU_F[1](require output Low when MCU is normal and PS=0) • When Cooperate with Aurix MCU SMU, 10KΩ pull down to GND; • When used as Digital input for wakeup capability, IO3 voltage cannot exceed 8V;	Open/ 5.1KΩ resistor pull down to GND
VPU_FS	22	O	Pull up for FS1B	• Rpd and Cpd connected to this pin will determine back up delay time of FS1B.	Open
RSTB	24	I/O	Reset	• RSTB is OD internal, need 5.1KΩ pull up to VDDIO. • 1.0nF capacitor used to robust against ESD GUN test up to ±8kV, place this capacitor close to RSTB pin. • RSTB is connect to MCU Reset	N/A
INTB	29	O	Interrupt	• Internal pull up to VDDIO, no need external Pull up source.	Open
Select	31	I	Configuration pin	• Resistor value in select pin determines Vcca / Vaux voltage. • Pull down to GND through resistor (Deep Fail Safe enabled); pull up to Vpre through resistor (DFS disabled)	N/A
Vaux, Vaux_E, Vaux_B	38,39,40	I/O	Vaux Regulator	• When Vaux used, must connect external PNP • Vaux connect to PNP-C and output capacitor, Vaux_B connect to PNP-B, Vaux_E connect to PNP-E. • Vaux output capacitor voltage tolerance should be>40V when Vaux is used as off board power supply	VAUX Open, Vaux_E Open, Vaux_B Open
Vcca, Vcca_E, Vcca_B	41,42,43	I/O	Vcca Regulator	• When external PNP used, Vcca connect to PNP-C and output capacitor, Vcca_B connect to PNP-B, Vcca_E connect to PNP-E. • When internal PNP used, Vcca connect to output capacitor, Vcca_E connect to Vpre, Vcca_B open.	N/A
GATE_LS	44	O	Gate Driver	• When GATE_LS pin connect to GND, Vpre is configured as Buck Mode; • When GATE_LS pin connect to Gate of MOS, Vpre is configured as Buck-Boost Mode,	N/A

FS45/FS65 POWER MANAGEMENT

QUESTIONS

- ***Vsup:*** *What's the Input range of the device and Work State ?*
- ***Vsup:*** *What's the function of Pi filter, how to select components for VSUP/Vsense ?*
- ***Vpre:*** *How to configure Buck only/ Buck-Boost Mode and how to design Vpre external circuits?*
- ***Vcore:*** *How to design Vcore external circuits and how to use FCRBM function?*
- ***Vcca/Vaux:*** *What's vaux connection when used or unused?*
- ***Vcca/Vaux:*** *What's Vcca connection when 100mA/300mA current capability?*
- ***Vcca/Vaux:*** *How to configure VCCA/VAUX voltage level?*
- ***Vcca/Vaux:*** *How to use Tracker Mode and what's the advantage?*
- ***Vcca/Vaux:*** *What's the behavior of Vcca/Vaux when overcurrent happen and how to recovery ?*
- ***Vcore/Vcca/Vaux:*** *What's degrade mode and how to configure it?*
- ***Vkam:*** *What's Vkam, how to configure Vkam?*

VSUP: WHAT'S THE INPUT RANGE OF THE DEVICE AND WORK STATE ?

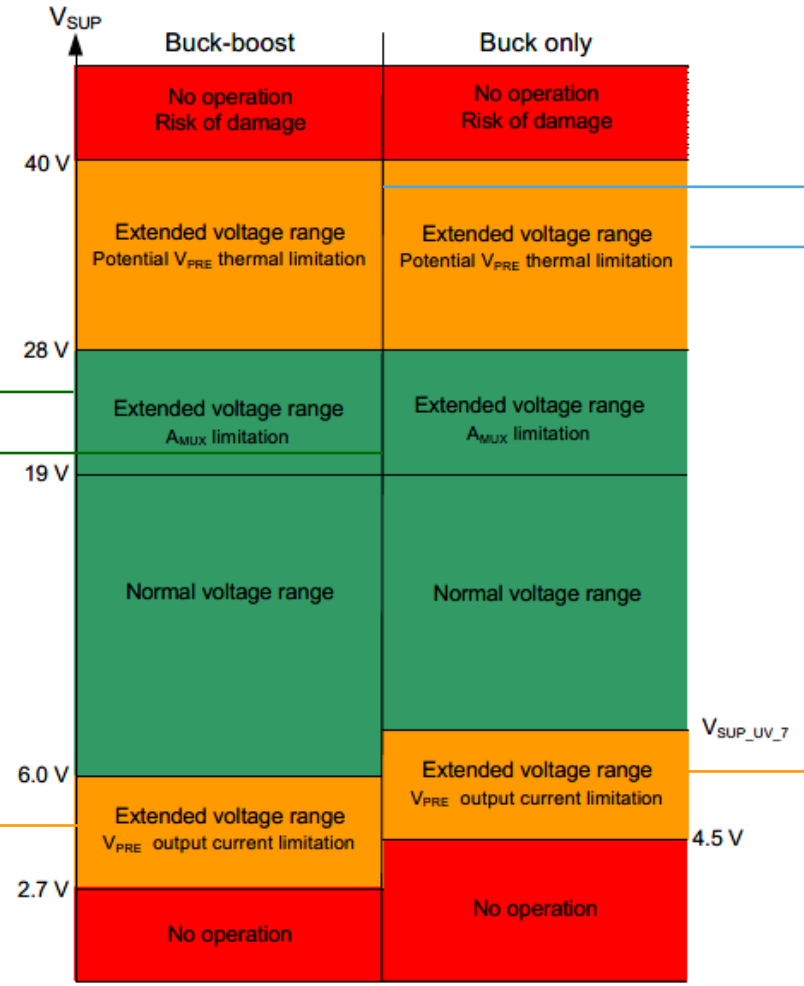


Figure 32. Input voltage range

❖ ***VPRE BUCK-BOOST & BUCK only Mode***

- *VSUP> 19 V: Mux_out limitation*
- *VSENSE and IO_0 maximum analog input voltage range is 19 V. Internal 2.5 V reference voltage accuracy degraded.*

❖ ***VPRE BUCK-BOOST & BUCK only Mode***

VSUP > 28 V: Potential VPRE thermal limitation RDS(on) , Current limitation and overcurrent detection are specified for VSUP< 28 V.

❖ ***VPRE BUCK-BOOST Mode***

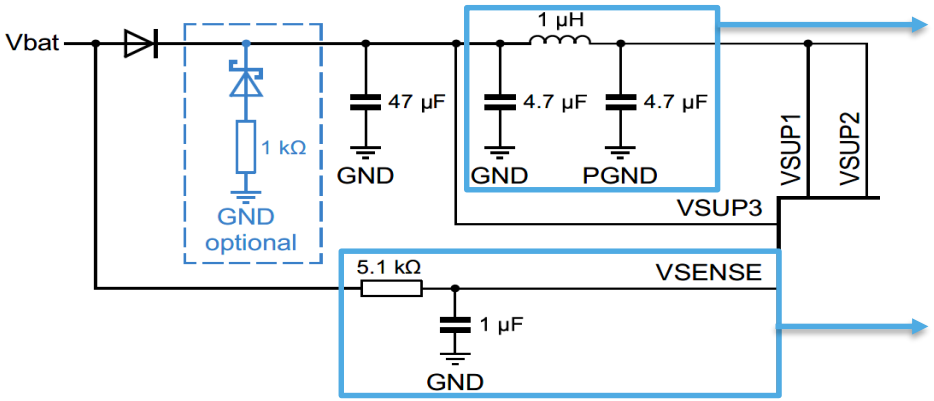
- *VSUP > VSUP_UV_5(5.6V Max) when battery power rising, device power up.*
- *VSUP< VSUP_UV_L(2.7V Max) when battery power falling, device power down.*
- *VPRE output current capability limited during Vsup=2.7V~6V.*

❖ ***VPRE BUCK only Mode***

- *VSUP > VSUP_UV_5(5.6V Max) when battery power rising, device power up.*
- *VSUP< VSUP_UV_L_B(4.5V Max) when battery power falling, device power down.*
- *VPRE output current capability limited during Vsup=4.5V~Vsup_uv_7.*
- *CAN communication is guaranteed for VSUP> 6.0 V. LIN communication stopped when VSUP< 7.0 V if LIN_J2602_DIS bit is not set.*
- *For VCCA and VAUX, 5.0 V configuration, undervoltage triggers at low VSUP(refer to VCCA_UV_5 and VAUX_UV_5)*

Note: If only Vsup > VSUP_UV_5(5.6V Max), Device will power on, regardless of IO pins state.

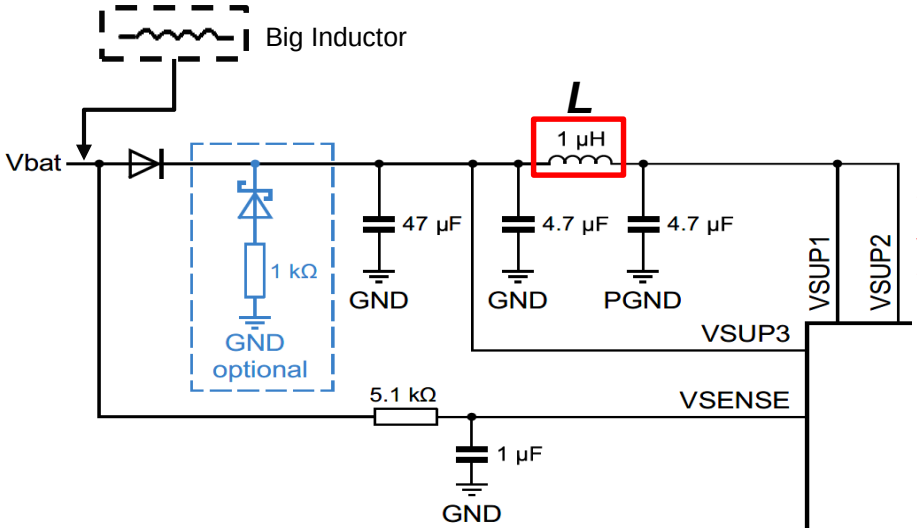
VSUP: WHAT'S THE FUNCTION OF PI FILTER, HOW TO SELECT COMPONENTS FOR VSUP/VSENSE ?



- **PI Filter Function:**

1. *PI filter will filter the noise from Vbat to Vsup1/2, avoid the noise impaction on SMPS.*
2. *PI filter will filter the noise from VSUP1/2(SMPS) to Vsup3, avoid SMPS noise impaction on Vsup3.*

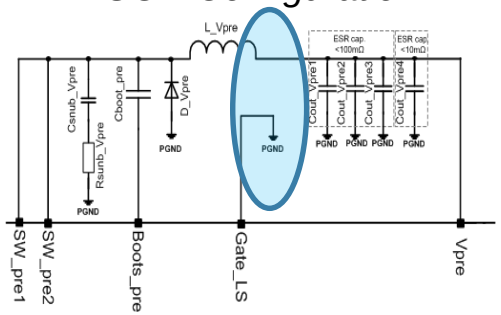
1. *A big capacitor >47uF is needed before Vsup3 for VBATT oscillation Robust.*
2. *Vsense pin should connect prior to Reverse Protection circuit, so that sense battery voltage.*
3. *Vsense pin can stand -14V~40V voltage.*
4. *5.1KΩ resistor should NOT be changed, otherwise it will impact on AMUX output accuracy.*



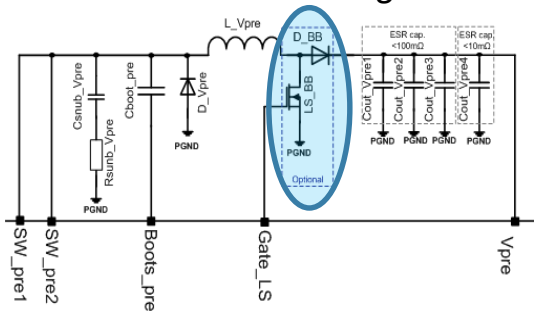
Note: Datasheet says, Vsup1/2 and Vsup3 should be the same power, so L<2.2uH to avoid voltage gap between Vsup1/2 and Vsup3 created when battery voltage oscillation. If needed, another inductor before FS45/FS65 for the whole board with a bigger value to help the EMC Performance.

VPRE: HOW TO CONFIGURE BUCK ONLY/ BUCK-BOOST MODE AND HOW TO DESIGN VPRE EXTERNAL CIRCUITS?

BUCK Configuration



BUCK-BOOST Configuration



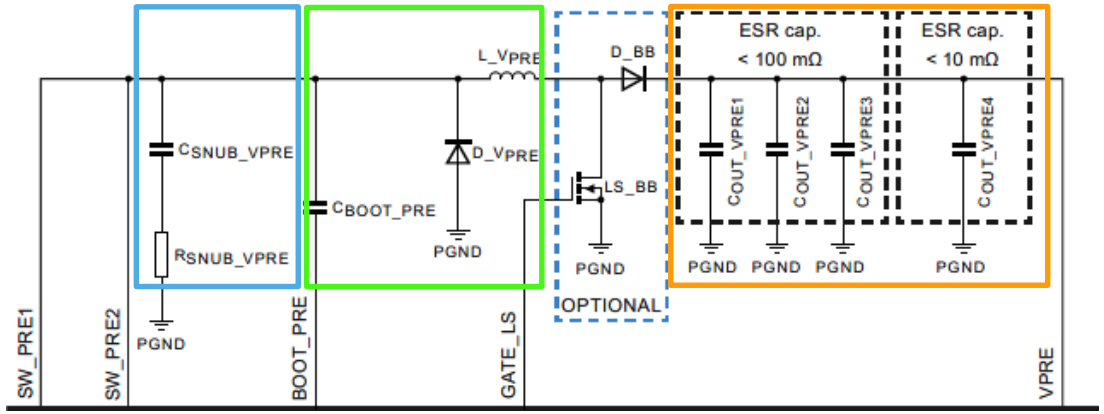
- *Vpre mode is automatically detected when Power up and wake up from LPOFF mode.*
- *After device power up, Vpre mode can be known by reading LS_DETECT bit in HW_CONFIG register.*

Table 34. HW_CONFIG register description

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	LS_DETECT	RESERVED	VCCA_PNP_DET	VCCA_HW	VAUX_HW	1	DFS_HW1	DBG_HW

Table 35. HW_CONFIG description and configuration of the bits (default value in bold)

LS_DETECT	Description	Report the hardware configuration of V_{PRE}
	0	Buck-boost
	1	Buck only
	Reset condition	Power on reset/refresh after LPOFF



Snubber for emission reduction:

- *Filter ripple at turn ON*
- *Values depends of PCB layout performance and should be fine tuned*
- *Resistor power dissipation must be bigger than 1/4W.*
- *Csnub_pre usually <2.2nF, Rsnub_vpre usually ~10ohm from experience, and the Values depends on SW_PRE waveform. Big capacitor will lead to loss of Vpre efficiency .*

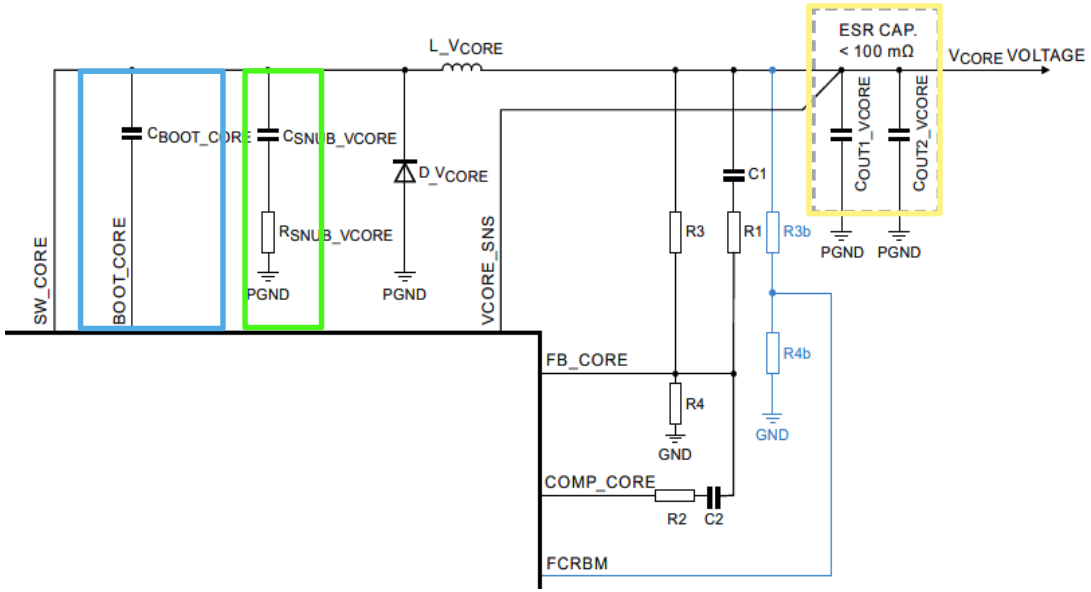
Bootstrap capacitor: 100nF

- *Provide High side gate drive at Vsup +10V,440KHZ switching frequency*
- *Not Recommended to add resister between CBOOT_PRE and BOOT_PRE pin.*

Output filtering capacitor :

- *Ceramic capacitor with low ESR. Minimum 40µF recommended.*
- *Low ESR <10mohms at resonance frequency.*
- *Voltage rating > 2x max output voltage (16V)*

VCORE: HOW TO DESIGN VCORE EXTERNAL CIRCUITS AND HOW TO USE FCRBM FUNCTION.



Snubber for emission reduction:

- *Filter ripple at turn ON.*
- *Values depends of PCB layout performance and should be fine tuned.*
- *Resistor power dissipation must be bigger than 1/4W.*
- *Csnub_core usually <2.2nF, Rsnub_coree usually ~10ohm from experience, and it depends on SW_CORE waveform. Big Capacitor will lead to lose of Vcore efficiency.*

Bootstrap capacitor: 100nF

- *Provide High side gate drive at Vsup +10V,2.2MHZ switching frequency*
- *Not Recommended to add resister between CBOOT_CORE and BOOT_CORE pin.*

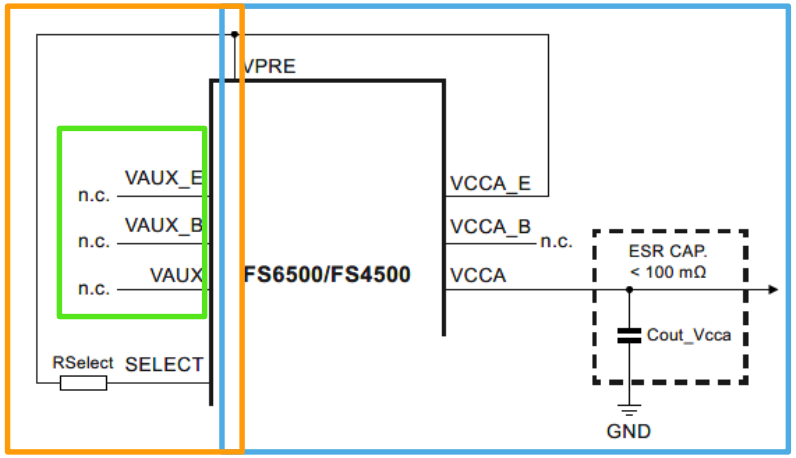
- *Ceramic output filtering capacitor from 20uF to 40uF depending on output current capability (low ESR)*
- *FB_CORE is always regulated at 0.8V and Vcore voltage Configurable from 1V to 5V range is setup by the external resistor bridge R3/R4 (+/-1%).*
- *FCRBM pin connect to the same resistor bridge with FB_CORE pin, when | FCRBM-FB_CORE | > 150mV, FCRBM_OV, FCRBM_UV Triggered; this function is used for Vcore external resistors(R3,R4) drift monitoring.*
- ***FCRBM_OV, FCRBM_UV Impact configuration is same with VCORE_FB_OV, VCORE_FB_UV impact configuration(in INIT_VCORE_OVUV_IMPACT register)***
- *If R3b, R4b/FCRBM are not used, FCRBM pin should connect to FB_CORE pin.*

VCCA/VAUX: WHAT'S VAUX CONNECTION WHEN USED OR UNUSED?
WHAT'S VCCA CONNECTION WHEN 100MA/300MA CURRENT CAPABILITY

Vaux unused:

- ***leave Vaux_E, Vaux_B, Vaux open.***
- ***Vaux_UV flag is set and cannot be cleared, VOTHERS_G bit is also set and cannot be cleared.***

Select pin pull up to Vpre: DFS disabled. RSelect Resistor decide Vaux/Vcca voltage level.



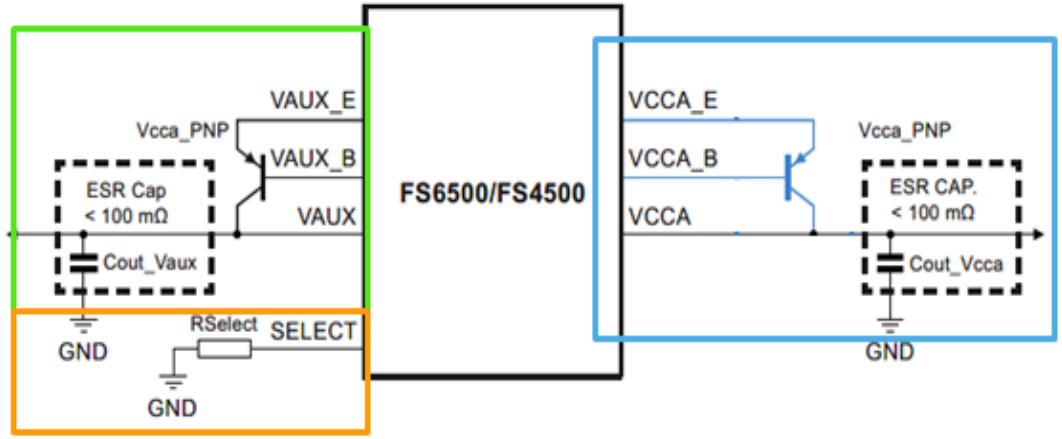
Vcca with internal PNP*:*

- *Vcca_E connect to Vpre, VCCA_B floating, VCCA pin connect to output capacitor.*
- *100mA current capability and 1% output accuracy.*

Vaux used: *400mA current capability.*

- ***Vaux pin can stand 40V max, so it can be used as off boards power supply.***
- ***Output capacitor: Min 4.7uF, 50V voltage tolerance when used as off-board power supply, as it is possible short to battery.***

Select pin pull down to GND: DFS enabled



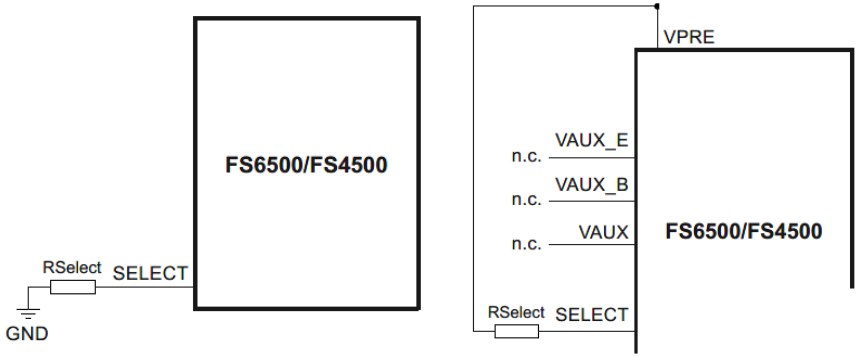
Vcca with external PNP:

- *300mA current capability with 3% accuracy.*

Note: Vaux can be used or unused, but Vcca must be used with internal PNP or external PNP Connection.

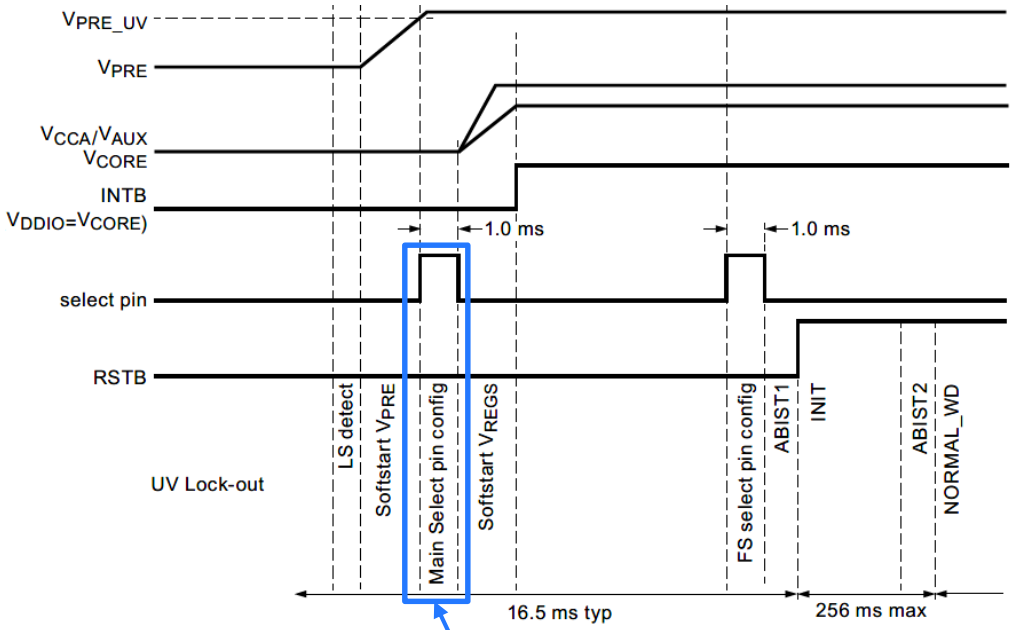
VCCA/VAUX: HOW TO CONFIGURE VCCA/VAUX VOLTAGE LEVEL

Vcca & Vaux output voltage are only decided by Rselect value as shown in below picture. No matter resistor connect to GND or Vpre.



Vcca	Vaux	Rselect (kΩ)	Recommended Value
3.3 V	3.3 V	< 6	5.1 kΩ ± 5 %
5 V	5 V	10.8 << 13.2	12 kΩ ± 5 %
3.3 V	5 V	21.6 << 26.4	24 kΩ ± 5 %
5 V	3.3 V	45.9 << 56.1	51 kΩ ± 5 %

Vcca & Vaux voltage is recognized once by reading resistor value in Main select pin configure phase.



NOTE:

- *If Rselect resistor value change after **Main Select pin config phase**, Vcca & Vaux voltage will not change and still output as detected in Main Select pin config phase.*
- ***If Rselect open, or short, or out of resistance ranges when detected in Main Select pin config phase. Both Vcca & Vaux will output 3.3V.***
- *Vcca & Vaux voltage level detection result can be SPI read in HW_CONFIG register, VCCA_HW and VAUX_HW bits.*

Vcca & Vaux voltage is configured by detecting Rselect value in this phase.

VCCA/VAUX: HOW TO USE TRACKER AND WHAT'S THE ADVANTAGE?

Vaux Tracker Mode Application:

1. *Vcca and Vaux are the same voltage level.*
2. *Vcca supply for ADC reference and Vaux supply for Ext Sensor.*

Advantage:

1. *Vaux can track Vcca voltage and keep ±15mV accuracy, will help to achieve high ADC sample accuracy.*
2. *Vaux pin can stand 40V DC Max, which protect pins in case battery short to Vaux through cable, so it is suitable for off boards power supply.*

How to configure Vaux as Tracker Mode

1. *Vaux is no tacking by default.*
2. *Tracker mode is enable by SPI writing VAUX_TRK_EN =1 in INIT_VREG Register(only can be Written in INIT Mode)*

VAUX_TRK_EN	Description	Configure VAUX regulator as a tracker of VCCA
	0	**NO tracking.**
	1	Tracking mode enabled and latched
	Reset condition	Power on reset

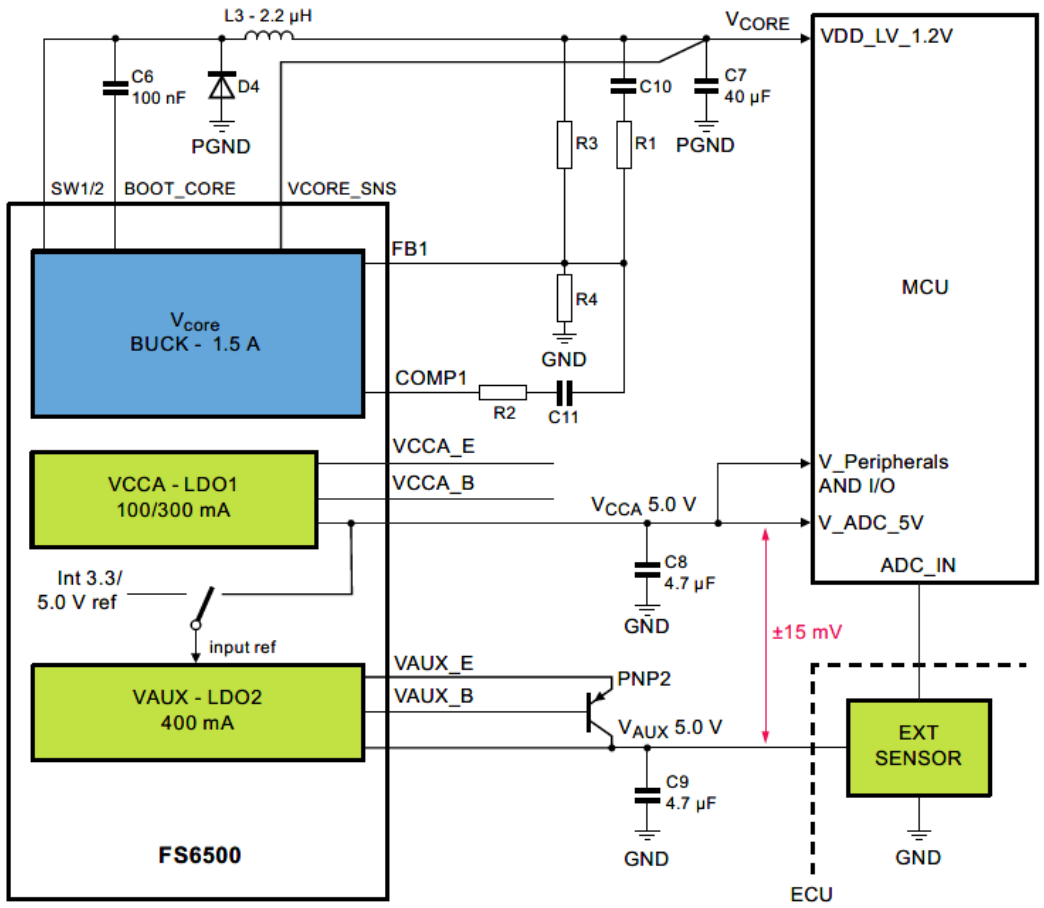


Table 22. INIT_VREG register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	0	1	P	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	0	TAUX_LIM_OFF	VAUX_TRK_EN	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	RESERVED	TAUX_LIM_OFF	VAUX_TRK_EN	BAT_FAIL

VCCA/VAUX: WHAT'S BEHAVIOR OF VCCA/VAUX WHEN OVERCURRENT HAPPEN AND HOW TO RECOVERY ?

- ***Vaux output Current Limit:*** *A current limitation is implemented to avoid uncontrolled power dissipation of the external PNP transistor. The current is limited to IAUX_LIM and the regulator is switch off after a dedicated duration tAUX_LIM_OFF under current limitation.*

I_{AUX_OUT}	V_{AUX} output current	—	—	400	mA
I_{AUX_LIM}	V_{AUX} output current limitation	400	—	800	mA
$I_{AUX\_LIM\_FB}$	V_{AUX} output current limitation foldback	60	—	240	mA
$V_{AUX\_LIM\_FB}$	V_{AUX} output voltage foldback threshold	0.6	—	1.2	V
t_{AUX_LIM}	V_{AUX} output current limitation filter time	1.0	—	3.0	µs
$t_{AUX\_LIM\_OFF1}$ $t_{AUX\_LIM\_OFF2}$	V_{AUX} output current limitation duration	10 50	— —	15 60	ms

Vaux_LIM_OFF (50ms by default) *is selected in INIT_VREG register.*

Table 22. INIT_VREG register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	0	1	P	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	0	TAUX_LIM_OFF	VAUX_TRK_EN	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	RESERVED	TAUX_LIM_OFF	VAUX_TRK_EN	BAT_FAIL

- ***Vaux is shut down and cannot recover*** *when Vaux output current reach current limit even if Vaux overcurrent removed. Vaux can be enabled by SPI writing "Vaux_EN=1" in REG_MODE Register.*

Table 60. REG_MODE register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	0	P	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RESERVED	RESERVED	RESERVED	RESERVED	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN

Vcca output Current Limit:

- ***Vcca use external PNP:*** *Vcca current limit protection mechanism is the same with Vaux.* ***Vcca shut down when output current reach current limitation and will not recover when overcurrent removed.*** *Vcca can be enabled by SPI writing "Vcca_EN=1" in REG_MODE Register.*

$I_{CCA\_LIM\_INT}$	V_{CCA} output current limitation (int. MOSFET)	100	—	675	mA
$I_{CCA\_LIM\_OUT}$	V_{CCA} output current limitation (external PNP)	300	—	675	mA
$I_{CCA\_LIM\_FB}$	V_{CCA} output current limitation foldback	60	—	240	mA
$V_{CCA\_LIM\_FB}$	V_{CCA} output voltage foldback threshold	0.6	—	1.2	V
t_{CCA_LIM}	V_{CCA} output current limitation filter time	1.0	—	3.0	µs
$t_{CCA\_LIM\_OFF1}$ $t_{CCA\_LIM\_OFF2}$	V_{CCA} output current limitation duration	10 50	— —	15 60	ms

Vcca_LIM_OFF (50ms by default) *is selected in INIT_VREG register.*

Table 22. INIT_VREG register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	0	0	0	0	1	P	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	0	TAUX_LIM_OFF	VAUX_TRK_EN	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	RESERVED	TAUX_LIM_OFF	VAUX_TRK_EN	BAT_FAIL

Table 60. REG_MODE register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	0	1	0	1	1	0	P	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	RESERVED	RESERVED	RESERVED	RESERVED	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN

- ***Vcca with internal PNP:*** *Vcca outputs 0 when Vcca output current reach to current limit,* ***Vcca will recover automictically after overcurrent current removed****.*

$I_{CCA\_LIM\_INT}$	V_{CCA} output current limitation (int. MOSFET)	100	—	675	mA
$I_{CCA\_LIM\_OUT}$	V_{CCA} output current limitation (external PNP)	300	—	675	mA
$I_{CCA\_LIM\_FB}$	V_{CCA} output current limitation foldback	60	—	240	mA
$V_{CCA\_LIM\_FB}$	V_{CCA} output voltage foldback threshold	0.6	—	1.2	V

VCORE/VCCA/VAUX: WHAT'S DEGRADE MODE AND HOW TO CONFIGURE IT?

- *Vcore, Vcca, Vaux support degrade mode, only valid when they output 5V. Degrade mode has a lower UV voltage threshold.*

$V_{CCA\_UV\_5}$	V_{CCA} undervoltage detection threshold (5.0 V configuration)	4.5	—	4.75	V
$V_{CCA\_UV\_5D}$	V_{CCA} undervoltage detection threshold (degraded 5.0 V)	3.0	—	3.2	V
$V_{CORE\_FB\_UV}$	V_{CORE} FB undervoltage detection threshold	0.67	—	0.773	V
$V_{CORE\_FB\_UV\_D}$	V_{CORE} FB undervoltage detection threshold - degraded mode	0.45	—	0.58	V
$V_{AUX\_UV\_5}$	V_{AUX} undervoltage detection threshold (5.0 V configuration)	4.5	—	4.75	V
$V_{AUX\_UV\_5D}$	V_{AUX} undervoltage detection threshold (degraded 5.0 V)	3.0	—	3.2	V

- *Vcore, Vcca, Vaux are normal mode by default and degraded mode can be configured by MCU SPI writing INIT_SUPERVISOR register. (only can be written in INIT_FS mode).*

Table 80. INIT_SUPERVISOR register description

Write																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	1	1	0	0	0	1	1	P	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_RANGE	Secure_3	Secure_2	Secure_1	Secure_0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_RANGE

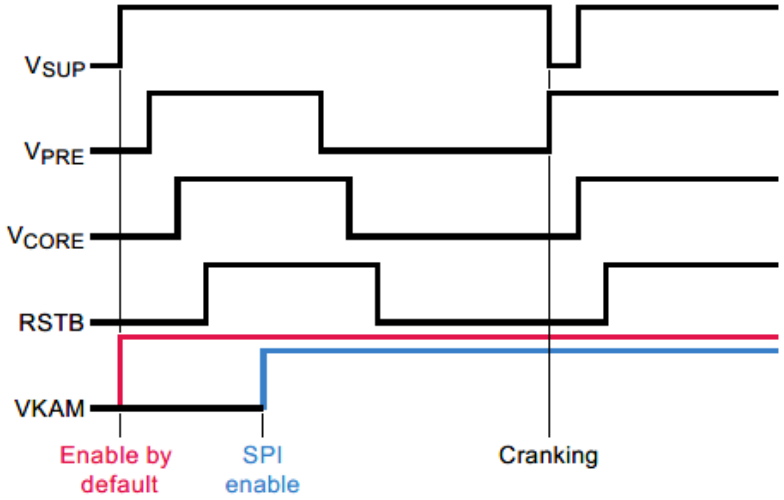
Note: ABIST2_Vaux is conducted through MCU SPI command, ABIST2_VAUX must be conducted before Vaux degraded mode configuration, otherwise, ABIST2_VAUX will fail.

VKAM: WHAT'S VKAM, HOW TO CONFIGURE VKAM ?

- *VKAM is an always ON regulator once it is enabled, no matter in LPOFF or DFS mode(Powered by VSUP3). VKAM spec are shown as below:*

VKAM voltage regulator					
V_{KAM}	V_{KAM} output voltage	3.0	3.5	4.0	V
I_{KAM_OUT}	V_{KAM} output current	—	—	3.0	mA
I_{KAM_LIM}	V_{KAM} output current limitation	4.0	—	10.0	mA
I_{SUP_KAM}	V_{KAM} current consumption from V_{SUP3} • I_{KAM_OUT} = 0 mA • I_{KAM_OUT} < 1.0 mA • 1.0 mA < I_{KAM_OUT} < 3.0 mA	 — — —	 — — —	 25 150 2.15	 µA µA mA

- *VKAM and IO5 use the same pin, for MC33FS6504LAE(ASIL D) and MC33FS6514LAE(ASIL D), VKAM is ON by default; VKAM should be enabled by SPI command(VKAM_EN=1 in Mode Register in Normal Phase) for other FS part numbers.*



FS45/FS65 SYSTEM FUNCTION

QUESTIONS

- ***MUX_OUT:*** *What's MUX_OUT and HOW to use MUX_OUT ?*
- ***MUX_OUT:*** *MUX_OUT accuracy and how to calibration ?*
- ***LDT:*** *What is LDT ? How to use LDT? What's LDT accuracy ? How to do calibration ?*
- ***SPI:*** *What's FS45/FS65 SPI prototype ? How to configure the parameter in software?*
- ***IOs:*** *What function IO0 can support and how to use the function ?*
- ***IOs:*** *What function IO2&IO3 can support and how to use the function ?*
- ***IOs:*** *What function IO4&IO5 can support and how to use the function ?*
- ***CAN:*** *How CANH/CANL short to battery, CANH/CANL short to GND detection?*
- ***CAN:*** *FS45/FS65 CAN PHY work normally in DEBUG mode, but fail after changing to non-DEBUG Mode?*

MUX_OUT: WHAT'S MUX_OUT, HOW TO USE MUX_OUT ? MUX_OUT ACCURACY AND HOW TO DO CALIBRATION ?

- *MUX_OUT pin delivers analog voltage to the MCU ADC input. Help customer save ADC Sample circuits.*
- *Monitoring battery voltage from vsense, FS45/FS65 internal temp, and so on. Analog voltage can be selected from Vsense, IO0, IO5/VKAM, Internal 2.5V or Internal temp sensor. MUX Input Channels and Ratios are selected by SPI writing IO_OUT_AMUX register AMUX_2:0 Bits.*

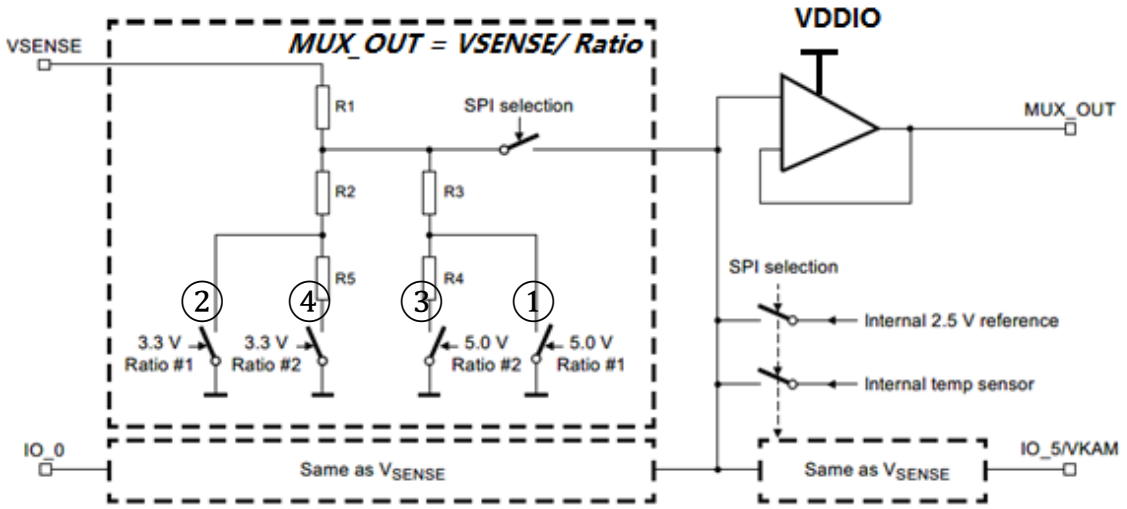
When AMUX_2:0 select Vsns, IO0, IO5

MUX_OUT = Vsense/Ratio; Ratio is selected by wide range or tight range.

	Description	Select AMUX output
AMUX_2:0	**000**	V_{REF}
	001	V_{SNS} wide range
	010	IO_0 wide range
	011	IO_5 wide range
	100	V_{SNS} tight range
	101	IO_0 tight range
	110	IO_5 tight range/VKAM
	111	Die Temperature Sensor
	Reset condition	Power on reset

there are both wide ranges/tight ranges @VDDIO=3.3V or VDDIO=5V.

$V_{AMUX\_TG\_5}$	Divider ratio	(tight input voltage range) at V_{DDIO} = 5.0 V	—	2.0	① —
$V_{AMUX\_TG\_3P3}$	Divider ratio	(tight input voltage range) at V_{DDIO} = 3.3 V	—	3.0	② —
$V_{AMUX\_WD\_5}$	Divider ratio	(wide input voltage range) at V_{DDIO} = 5.0 V	—	5.0	③ —
$V_{AMUX\_WD\_3P3}$	Divider ratio	(wide input voltage range) at V_{DDIO} = 3.3 V	—	7.0	④ —



Configuration:

- *When AMUX_2:0 = 001(Vsns wide range), MUX_OUT = Vsense/Ratio, Ratio = 5 @ VDDIO=5V, Ratio = 7 @VDDIO=3.3V.* ***MUX_OUT voltage will not exceed VDDIO.***
- *When AMUX_2:0 = 100(Vsns tight range) MUX_OUT = Vsense/Ratio, Ratio = 2 @ VDDIO=5V, Ratio = 3 @VDDIO=3.3V.* ***MUX_OUT voltage will not exceed VDDIO.***
- *Same calculation when AMUX_2:0 select IO0 analog input, IO5 analog input.*
- ***VSENSE and IO_0 maximum analog input voltage range is 19 V.***
- *Serial Resistors(R1,R2,R3,R4,R5) are MΩ level.*

Calibration:

VSENSE voltage can be monitored through the MUX_OUT pin with ***5.0 %*** *accuracy, After calibration, the VSENSE monitoring accuracy can achieve* ***±1%,*** *for both VDDIO = 3.3 V and 5.0 V, in wide range resistor bridge configuration (without taking into account the VSENSE supply accuracy used for the calibration). Calibration method example:*

- *Set VBAT1 = 12V, MCU ADC read MUX_OUT output voltage as Vmux1 ;*
- *Set VBAT1 = 14V, MCU ADC read MUX_OUT output voltage as Vmux2 ;*

  *VBAT1 = A*Vmux1 + B;*

  *VBAT2 = A*Vmux2 + B;*
- *get A. B, calculate Vsense voltage by Vsense = A* Vmux+ B.*

MUX_OUT: WHAT'S MUX_OUT, HOW TO USE MUX_OUT ? MUX_OUT ACCURACY AND HOW TO CALIBRATION ?

- ***When AMUX_2:0 select internal 2.5V reference***

MUX_OUT = 2.5V, Internal 2.5 V reference voltage accuracy degraded when VSUP > 19 V.

V_{AMUX_REF1}	Internal voltage Reference with 6.0 V < V_{SUP} < 19 V	2.475	2.5	2.525	V
V_{AMUX_REF2}	Internal voltage reference with V_{SUP} ≤ 6.0 V, or V_{SUP} ≥ 19 V	2.468	2.5	2.532	V

- ***When AMUX_2:0 select internal 2.5V reference***

Internal temp sensor, real temperature can be calculated by below formula, VMUX is FS45/FS65 MUX_OUT voltage read by MCU ADC.

$$T(°C) = (V_{AMUX} - V_{AMUX\_TP})/V_{AMUX\_TP\_CO} + 165$$

$V_{AMUX\_TP\_CO}$	Internal temperature sensor coefficient	—	9.9	—	mV/°C
V_{AMUX_TP}	Temperature sensor MUX_OUT output voltage (at T_J = 165 °C)	2.08	2.15	2.22	V

LDT: WHAT IS LDT ? HOW TO USE LDT? WHAT'S LDT ACCURACY ? HOW TO DO CALIBRATION ?

- *Long duration timer(LDT), with an integrated oscillator. The timer is configurable by the SPI and can operate in normal mode and low-power mode. 2 time bases: 1s or 488uS, configured by SW register bits. The longest timer is 194 days with 1s time base.*

	Osc freq	Osc period	Prescaler	Counter resolution	Max count	
Operation	32768 Hz	30.52 µs	16 x 2048	1 s	4660 Hrs	194 days
Calibration	32768 Hz	30.52 µs	16	488 µs	8192 s	2.28 Hrs

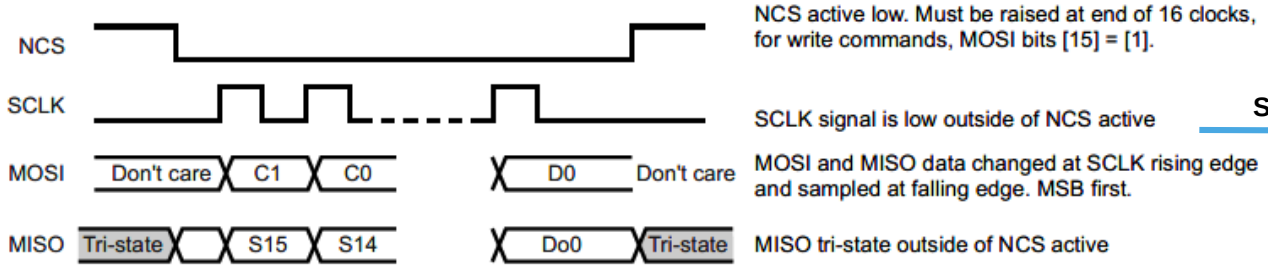
→ ***LONG_DURATION_TIMER register,*** *MODE bit = 1 (default)*

→ ***LONG_DURATION_TIMER register,*** *MODE bit = 0*

- *Long duration timer(LDT) accuracy: Statistical analysis shows the ±5.0 % oscillator accuracy, After calibration, accuracy could achieve ±2.0 % from –20 °C to 85 °C temperature. Calibration method is in* ***Page 71*** *of FS45/FS65 Datasheet V7.0.*
- *Long Duration Timer have 5 Modes, detailed description is in* ***Page 72, Page 73*** *of FS45/FS65 Datasheet V7.0.* ***Function 4 can be used as periodical wake-up system checking when system is in LPOFF mode.***
- *LDT function 5 principle(software flow) is shown in* ***Page 36*** *of NXP AN5238 V7.0.*
- *LDT diagnostic verify the correct operation of the LDT and wake-up by LDT in case it is used as a safety function. It is described in* ***Page 37&Page38*** *of NXP AN5238 V7.0.*

SPI: WHAT'S FS45/FS65 SPI PROTOTYPE ? HOW TO CONFIGURE THE PARAMETER IN SOFTWARE?

- **FS45/FS65 SPI Driver configuration.**



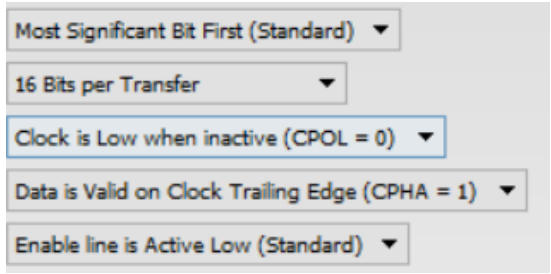
NCS active low. Must be raised at end of 16 clocks, for write commands, MOSI bits [15] = [1].

SCLK signal is low outside of NCS active

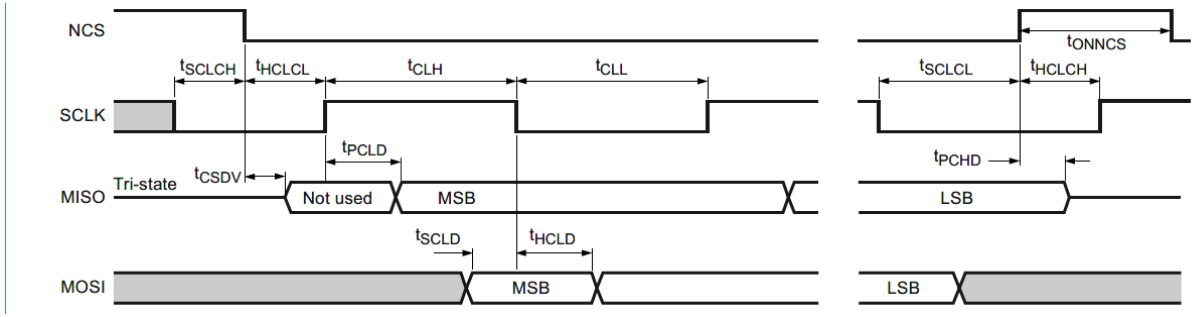
MOSI and MISO data changed at SCLK rising edge and sampled at falling edge. MSB first.

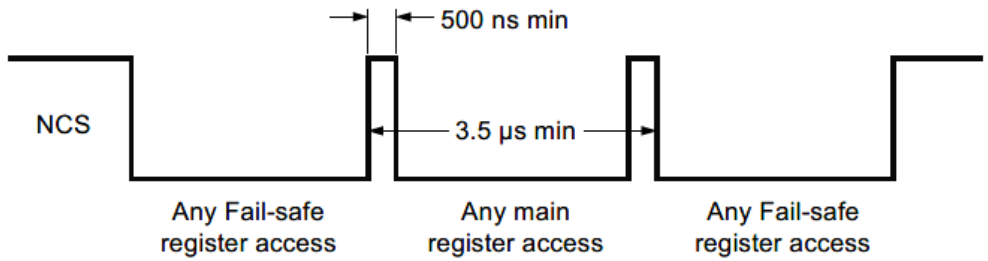
MISO tri-state outside of NCS active

SPI driver Configuration



- **FS45/FS65 SPI Timing**





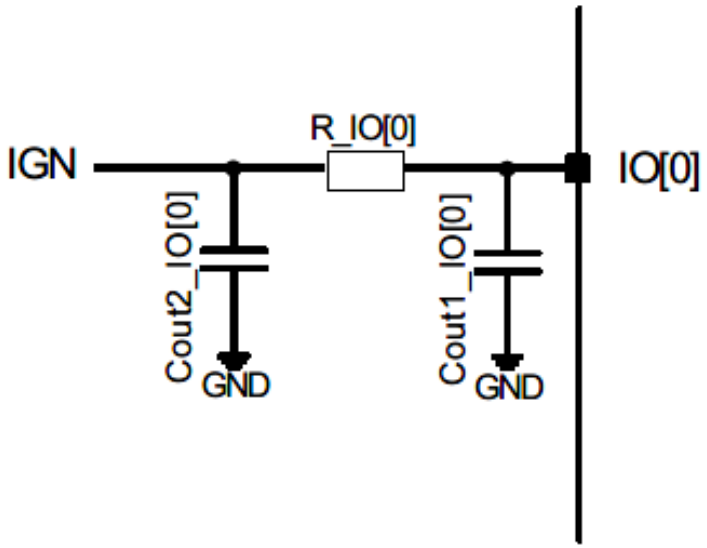
- *Detailed SPI timing, please refer to Page 22 of FS45/FS65 Datasheet.*
- *The minimum time between two NCS low sequences is defined by TONNCS= 500ns.*
- *Two consecutive accesses to the fail-safe registers must be done with a 3.5µs minimum NCS high time in between.*

IOS: WHAT FUNCTION IO0 CAN SUPPORT AND HOW TO USE THE FUNCTION ?

- *IOs have Multi-Function, "X" in below picture represents the function IO can support.*
- ***IO0** Support **Digital input wake up capability(default)** and **Analog input** function.*

Table 8. I/Os configuration

I/O number	Digital input wake-up capability	Analog input	Output gate driver	VKAM	FCCU monitoring	Ext. IC monitoring
IO_0	X	X				
IO_2	X				X	
IO_3	X				X	
IO_4	X		X			X
IO_5	X	X		X		X



(1) IO0 can support Digital Input Function (Wake up IO)

- *IO0 is wake up function by default, can wake up device when it is in LPOFF mode. Wake up source and wake up signals can be configured in INIT_WU1 register as below.*

Table 25. INIT_WU1 description and configuration of the bits (default value in bold)

WU_IO0_1:0	Description	IO_0 wake-up configuration
	00	NO wake-up capability
	01	**Wake-up on rising edge - or high level**
	10	Wake-up on falling edge - or low level
	11	Wake-up on any edge
	Reset condition	Power on reset

- ***IO0 pin max rating is 40V, IO0 is always recommended to connect to Ignition of the car.***
- *IO0 circuit is shown as below, Cout2_IO[0] is used to against ESD GUN test up to ±8.0 kV, R_IO[0] and a capacitor Cout1_IO[0] to limit the current and the negative voltage during the high transient pulse on the line. Please see details in **AN5238-5.5 IO_0 ignition connection.***
- ***Only IO0 Low to High transition can wake up device from Deep fail safe mode.***
- *Valid high/ low voltage: IO0 pin Voltage>2.6V = High, Voltage <2.1V = Low.*
- *Wake up signal delight time:*

t_{WU_GEN}	General wake-up signal deglitch time (for any wake-up signal on IOs)	60	70	80	µs

(2) Analog Input Function

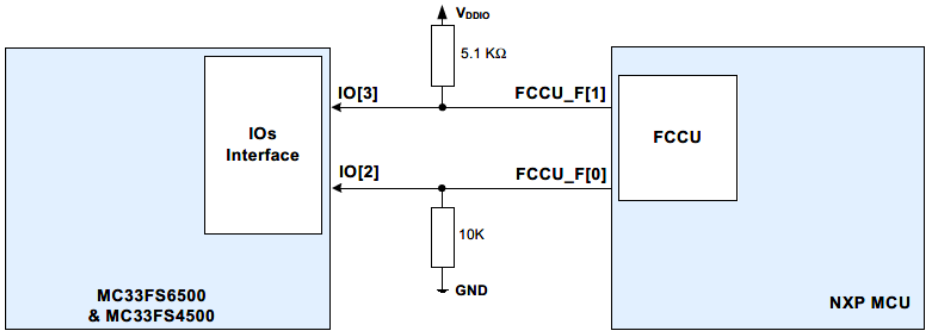
- ***IO0 is always used as wake up function, when used as analog input function, it support 19V max input.***

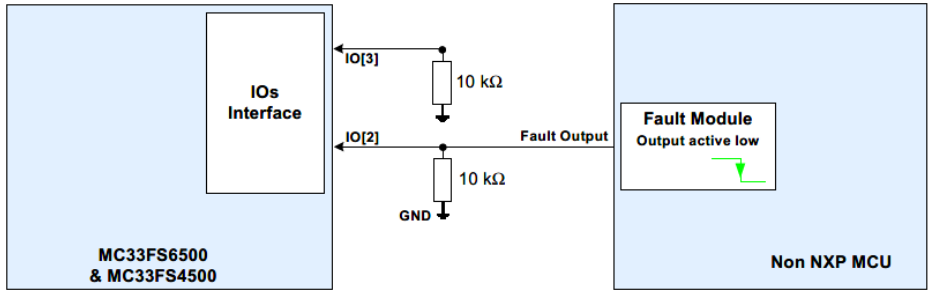
IOS: WHAT FUNCTION IO2&IO3 CAN SUPPORT AND HOW TO USE THE FUNCTION ?

- *IOs have Multi-Function, "X" in below picture represents the function IO can support.*
- ***IO2&IO3** Support **Digital input wake up capability** and **FCCU** function.*
- ***IO2,IO3 are FCCU monitoring by default. The function can only be disabled in INIT_FS mode.***

Table 8. I/Os configuration

I/O number	Digital input wake-up capability	Analog input	Output gate driver	VKAM	FCCU monitoring	Ext. IC monitoring
IO_0	X	X				
IO_2	X				X	
IO_3	X				X	
IO_4	X		X			X
IO_5	X	X		X		X





(1) FCCU:** when MCU detected error, it output unnormal FCCU/Fault signals to SBC IO2&IO3, SBC will reset MCU and assert FS0B=0 to make the system go to safe state. **IO2/IO3 are FCCU safety pins by default, Polarity is PS=0 by default, If IO2/IO3 are not used, IO_23_FS bit must be configured to 0 in INIT_FSSM register during INIT_FS mode.

IO_23_FS	Description	Configure the couple of IO_3:2 as safety inputs for FCCU monitoring
	0	Not safety
	1	**Safety critical**
	Reset condition	Power on reset
PS	Description	Configure the F_{CCU} polarity
	0	**Fccu_eaout_1:0 active high**
	1	Fccu_eaout_1:0 active low
	Reset condition	Power on reset

- *Hardware connection is shown as the picture left for NXP or Non NXP MCU with PS=0.*
- ***PS=0 Polarity means:***
  *(1) When IO[2]=**High**, IO[3] =**Low**, FCCU is normal. NO Reset toggled and FS0B is High. In this case, MCU should output **FCCU_F[1]=Low** and **FCCU_F[0]=High when MCU is normal.***
  (2) When IO[2], IO[3] are other states, SBC will Reset MCU and assert FS0B =0.
- ***SBC IO2&IO3 FCCU monitoring function only valid in Normal_WD phase(as soon as first good SBC watchdog refresh).***
- ***If SBC monitored FCCU error, customer can read the fault in DIAG_SF_IOs register:IO_23_FAIL bit.***

(2) IO2, IO3 used as digital input wake up capability

- *Configure IO_23_FS=0 No safety related & configure IO2,IO3 wake up type in INIT_WU1 register.*
- *Hardware connection is same with IO0 wake up circuit.*
- ***IO2&IO3 pins are 8V at max, so wake up voltage in IO2 and IO3 must not exceed 8V.***

IOS: WHAT FUNCTION IO4&IO5 CAN SUPPORT AND HOW TO USE THE FUNCTION ?

- *IOs have Multi-Function, "X" in below picture represents the function IO can support.* ***IO4 and IO5 are no wake up capability by default.***
- ***IO4*** *Support* ***Digital input wake up capability, Analog input, output gate driver*** *function.*
- ***IO5*** *Support* ***Digital input wake up capability, Analog input, VKAM*** *function.*
- ***IO4&IO5*** *can be configured as* ***External IC monitoring function,*** ***it is disabled by default, it can be configured in INIT_FSSM register during INIT_FS mode.***

Table 8. I/Os configuration

I/O number	Digital input wake-up capability	Analog input	Output gate driver	VKAM	FCCU monitoring	Ext. IC monitoring
IO_0	X	X				
IO_2	X				X	
IO_3	X				X	
IO_4	X		X			X
IO_5	X	X		X		X

(1) When IO4 is used as digital input wake up capability

- *IO4 is used as no wake up by default, wake up function and type can be configured by writing INIT_WU1 register,* ***WU_IO4_1:0.***
- *Hardware connection is same with IO0 wake up circuit.*
- *IO4 pin is 40V max rating.*

IO4

(2) When IO4 is used as output gate driver function

- *Configure IO4 as no wake up capability in INIT_WU1 register,* ***WU_IO4_1:0 &*** *configure IO4 as output gate driver by* ***IO_OUT_AMUX register, IO_OUT_4_EN, IO_OUT_4*** *bits.*
- *IO4 gate driver capability is shown as below.*

V_{IO4_OH}	High output level at I_{IO4_OUT} = –2.0 mA	V_{PRE} – 1.5	—	V_{PRE}	V	
V_{IO4_OL}	Low output level at I_{IO4_OUT} = +2.0 mA	0.0	—	1.0	V	
$V_{IO4\_OUT\_SK}$ $V_{IO4\_OUT\_SC}$	Output current capability	2.0 —	— —	— –2.0	mA	

(1) When IO5 is used as digital input wake up capability

- *IO5 is used as no wake up by default, wake up function and type can be configured by writing INIT_WU1 register,* ***WU_IO5_1:0.***
- *Hardware connection is same with IO0 wake up circuit.*
- ***IO5 pin is 20V max rating.***

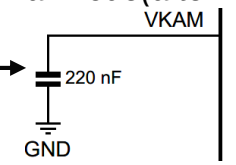
IO5

(2) When IO5 is used as Analog Input function (20V Max)

- *Configure IO5 as no wake up capability in INIT_WU1 register,* ***WU_IO5_1:0 &*** *configure IO5 as Analog Input by* ***write IO_OUT_AMUX register AMUX_2:0 Bits.***

(3) When IO5 is used as VKAM function.

- *Configure IO5 as no wake up capability in INIT_WU1 register& Configure* ***MODE*** *register VKAM_EN =1, this register can only be written in Normal Mode(after write INIT_INT register).*
- *Hardware connection is shown as*
- ***FS6504LAE&FS6514LAE IO5 is VKAM on by default.***

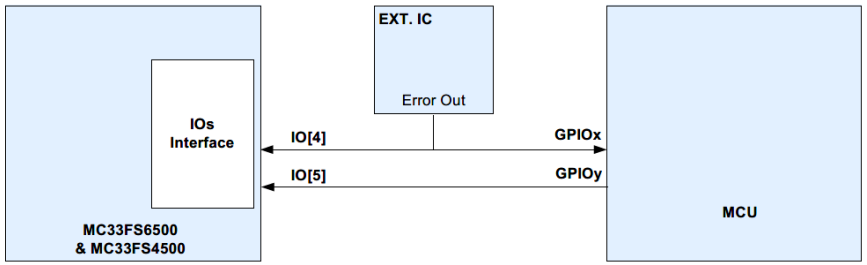


IOS: WHAT FUNCTION IO4&IO5 CAN SUPPORT AND HOW TO USE THE FUNCTION ?

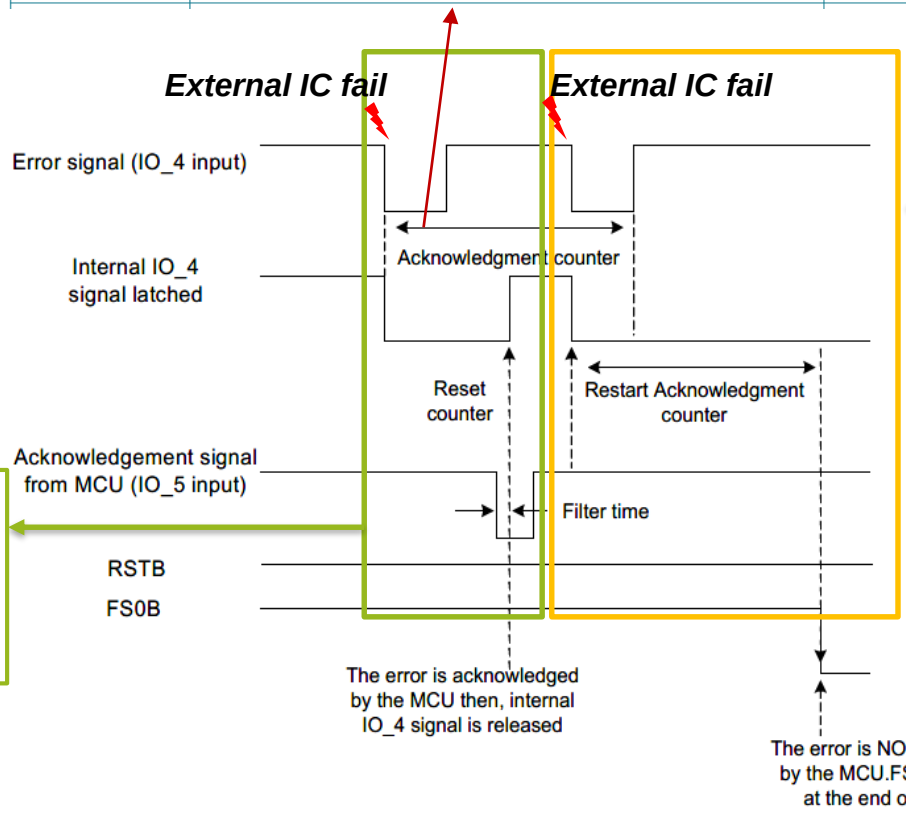
IO4&IO5 used as External IC monitoring Function (Safety Function)

IO4&IO5

- *IO4,IO5 are no wakeup capability by default and not safety related function by default, need configure INIT_FSSM Register IO_45_FS=1 to active external sensor monitoring function.*
- *Hardware Connection.*



t_{ACK_FS}	Acknowledgment counter (used for IC error handling IO_5)	7.0	—	9.7	ms



MCU did not send Low voltage to SBC IO5 within Acknowledge counter, when external IC fail(IO4 low), SBC will assert FS0B=0.

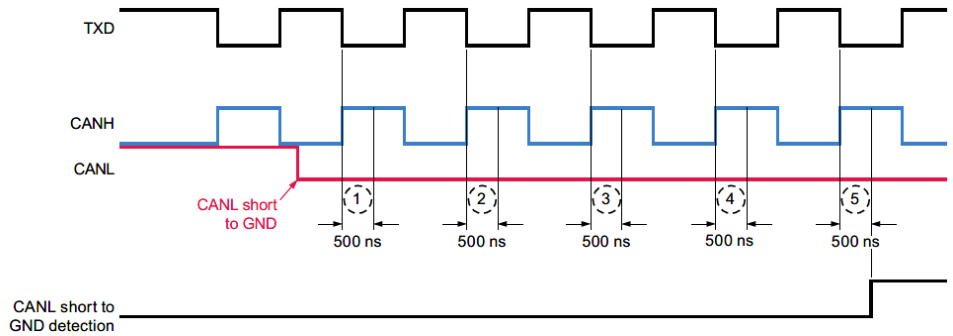
MCU detected External IC error and send Low voltage to SBC IO5 within Acknowledge counter, SBC will not assert FS0B=0.

CAN: HOW CANH/CANL SHORT TO BAT/GND DETECTED

CAN Diagnose function : CANH/CANL short to BATT/GND did not turn off CAN Transceiver.

Trigger condition:

1. ***CANL short to GND : VCANL pin voltage < 0.5V and 500 ns after TXD is activated low, and five consecutive times.*** ***0.5V is not threshold, the threshold is within 0V~0.5V, when CAN BUS short to GND, CANL short to GND may not reported as CANL did not low enough for diagnose due to voltage gap between CAN BUS and CANL pin.***



2. ***CANH short to BATT : VCANH pin voltage > 5.2V, 500 ns after TXD is activated low, and five consecutive times*****. 5.2V is not threshold, the threshold is within 0V~0.5V, when CAN BUS short to GND, CANL short to GND may not reported as CANL did not low enough for diagnose due to voltage gap between CAN BUS and CANL pin.***

3. ***CANL short to BATT : ICANH > 75mA(typ), 500 ns after TXD is activated low, and five consecutive times.*** ***There is usually chock between CANH/CANL and CAN BUS, so when CAN BUS short to BATT, ICANL<75mA and CANL Short to BATT cannot reported due to chock impaction.***

4. ***CANH short to GND : ICANL > 75mA(typ), 500 ns after TXD is activated low, and five consecutive times.*** ***There is usually chock between CANH/CANL and CAN BUS, so when CAN BUS short to BATT, ICANH<75mA and CANH Short to GND cannot reported due to chock impaction.***

CAN: FS45/FS65 CAN PHY work normally in debug mode, but fail after changing to non-debug mode?

Question: Some customer find FS45/FS65 CAN PHY can work normally in debug mode, but after change to NON-Debug Mode, FS45/FS65 CAN PHY cannot work.

Answer: This is mostly caused by unproper software configuration.

Check-List:

1. CAN_MODE_1:0 bits in CAN_LIN_MODE Register.

- In debug mode, FS65 CAN PHY is normal mode by default. So CAN PHY can work without software configuration.
- In non-debug mode, FS65 CAN PHY is sleep/wake-up capability mode by default, need software configure **CAN_MODE_1:0 = 11** in **CAN_LIN_MODE** register.

Table 65. CAN_LIN_MODE description and configuration of the bits (default value in bold)

CAN_MODE_1:0[1]	Description	Configure the CAN mode
	00	Sleep/no wake-up capability
	01	Listen only
	10	**Sleep/wake-up capability**
	11	Normal operation mode
	Reset condition	Power on reset

2. FS1B_CAN_IMPACT bits in INIT_FAULT Register.

- In debug mode, FS65 CAN PHY can work without considering FS1B pin state.
- In non-debug mode, FS65 CAN PHY mode will change to sleep/RX only(determined by CAN_DIS_CFG bit in INIT_WU2 register) when FS1B is Low, it is configured in **FS1B_CAN_IMPACT bits in INIT_FAULT Register.**

FS1B_CAN_IMPACT	Description	Configure CAN behavior when FS1B is asserted low
	0	No effect
	1	**CAN in RX only or sleep mode when FS1B is asserted (depends on CAN_DIS_CFG bit in INIT_WU2 register)**
	Reset condition	Power on reset

CAN_DIS_CFG	Description	Define CAN behavior when FS1B is asserted low
	0	**CAN in RX only mode (when FS1B_CAN_ IMPACT = 1 in INIT_FAULT register)**
	1	CAN in sleep mode (when FS1B_CAN_ IMPACT = 1 in INIT_FAULT register)
	Reset condition	Power on reset

FS45/FS65 STATE MACHINE AND MODES

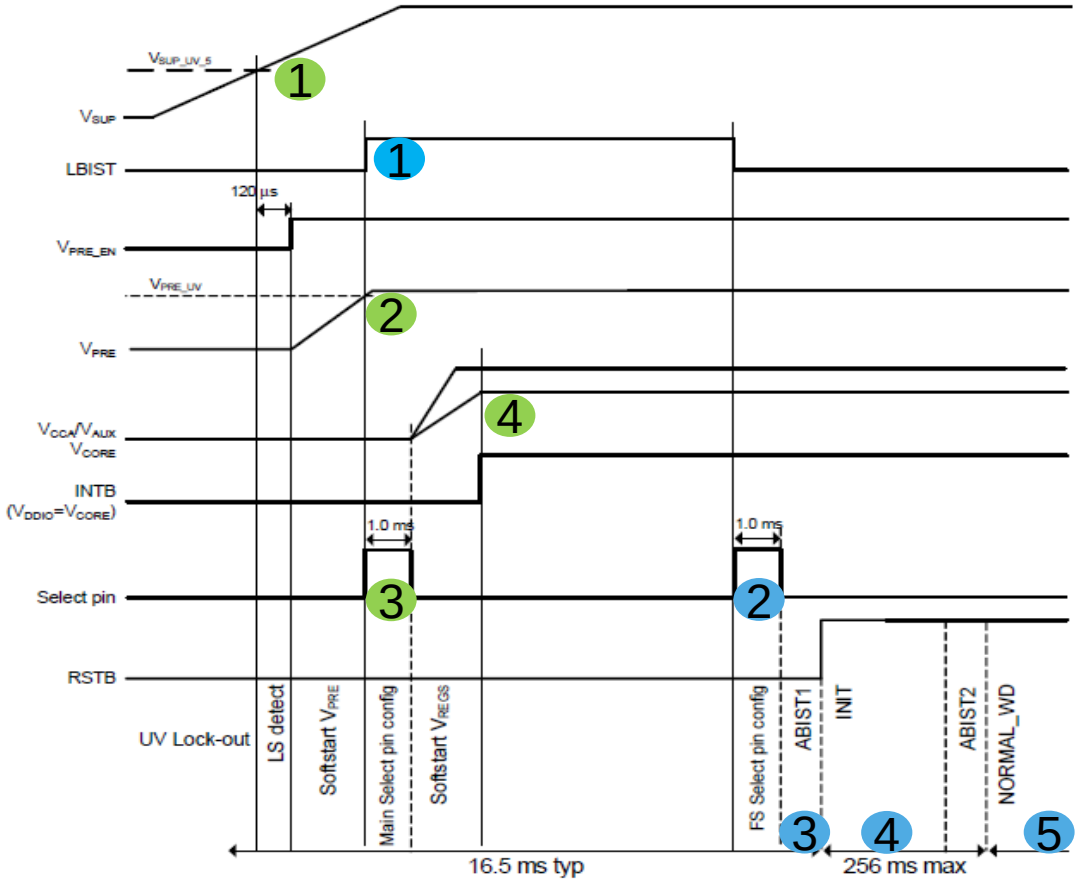
QUESTIONS

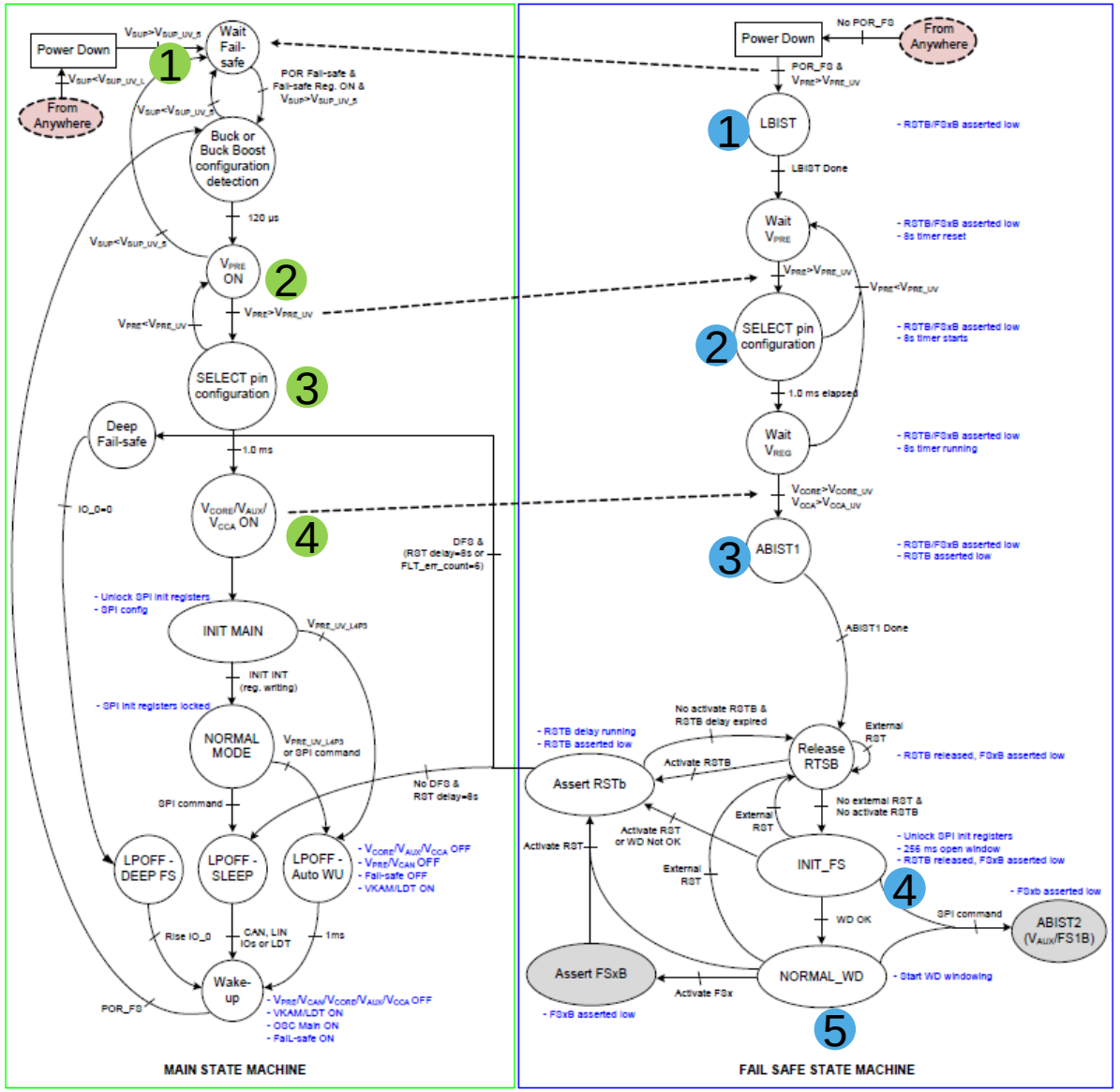
- ***State Machine:*** *How main state machine and Fail Safe state machine work ?*
- ***State Machine:*** *How FS45/FS65 state machine work with MCU ?*
- ***State Machine:*** *How to change main/fail safe machine state?*
- ***State Machine:*** *How state machine change when FS45/FS65 RSTB pin asserted to Low?*
- ***LPOFF/DFS Mode:*** *How to enter LPOFF/DFS and how to config DFS?*
- ***DEBUG Mode：*** *How to enter/exist Debug mode, what's special in debug mode ?*

STATE MACHINE: HOW MAIN STATE MACHINE AND FAIL SAFE STATE MACHINE WORK ?

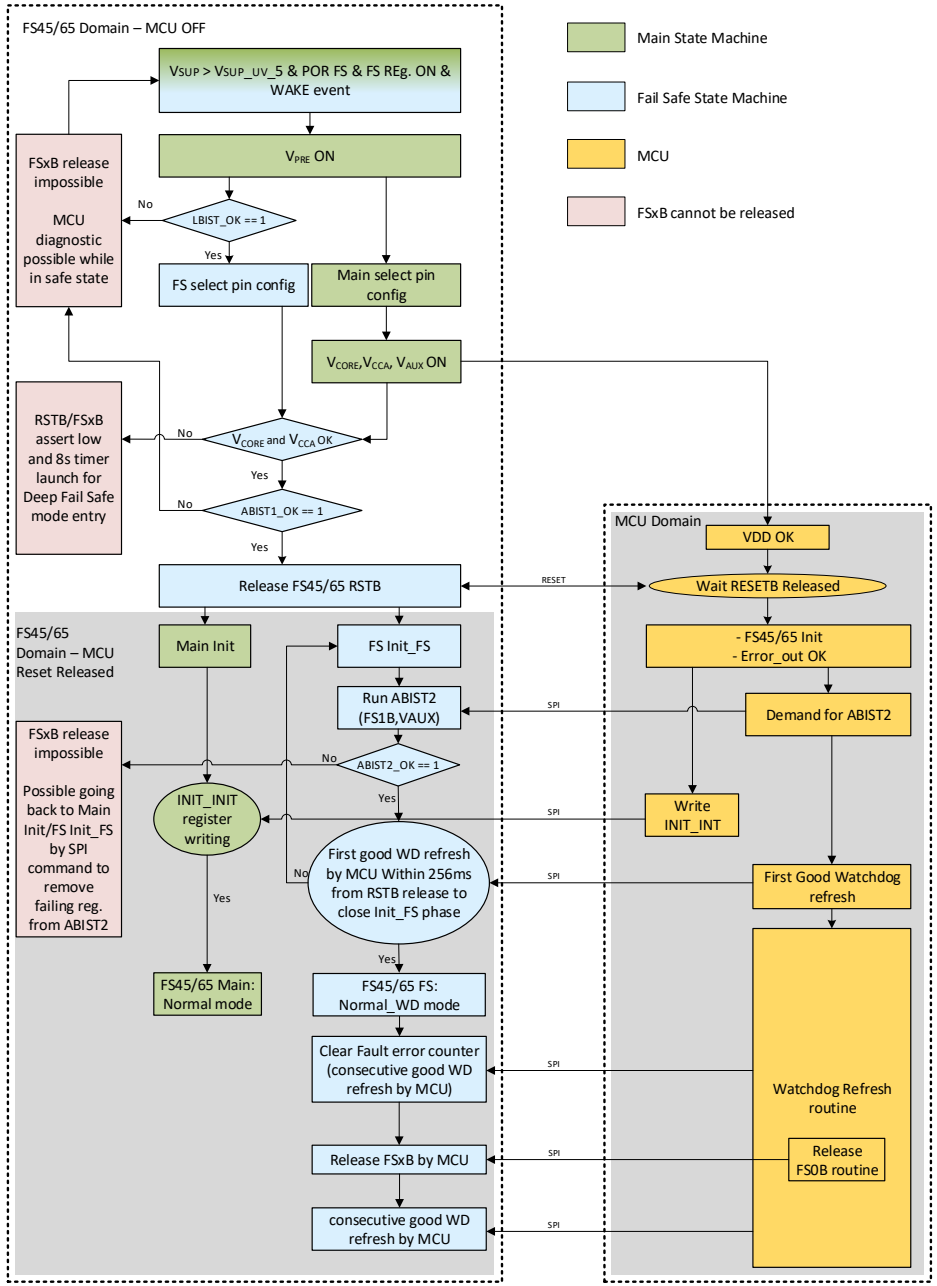
2 State machine work in parallel.

- *Main State Machine: Power Management;*
- *Fail Safe State Machine: Fail Safe Management.*





STATE MACHINE: HOW FS45/FS65 STATE MACHINE WORK WITH MCU



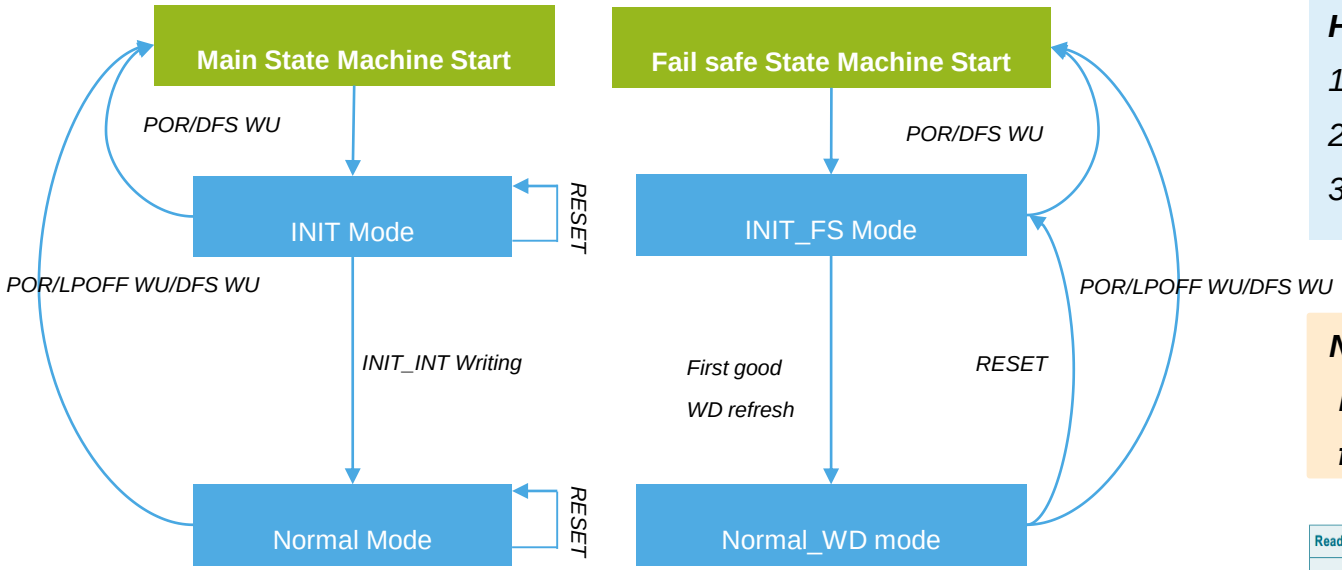
STATE MACHINE: HOW TO CHANGE MAIN/FAIL SAFE MACHINE STATE?

Main State Machine (there are INIT and Normal Mode)

- *Enter Normal Mode after SPI write INIT_INT Register.*
- ***Reset event in Normal Mode will not change Main State machine to INIT mode. All regulators can output normally.***
- *Re-enter INIT Mode after POR/wake-up from LPOFF or DFS*

Fail safe State Machine (there are INIT_FS and NORMAL_WD mode)

- ***Enter INIT_FS mode when Reset/POR/ wake-up from LPOFF or DFS.***
- *Enter NORMAL_WD mode after first good watchdog refresh.*



How state machine change when FS45/FS65 RSTB pin asserted to Low?

1. *All power rails(Vpre/Vcore/Vaux/Vcca/Vcan) output normally.*
2. *Main state machine mode did not change.*
3. *Fail safe State machine change to "INIT_FS" mode.*

Note: MODE Register show main state machine mode, not Fail safe state machine mode. When read Mode register and shows "Normal mode", fail safe state machine may be in INIT_FS mode or Normal_WD mode.

Read																
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
MISO	SPI_G	WU_G	CAN_G	LIN_G	IO_G	VPRE_G	VCORE_G	VOTHERS_G	VKAM_EN	RESERVED	RESERVED	RESERVED	INIT	NORMAL	DFS	LPOFF

Note: *Fail Safe State Machine did not work in LPOFF or DFS mode, so watchdog monitoring, OV/UV, FCCU monitoring did not work in LPOFF or DFS mode.*

LPOFF/DFS MODE: HOW TO ENTER LPOFF/DFS AND HOW TO CONFIG DFS

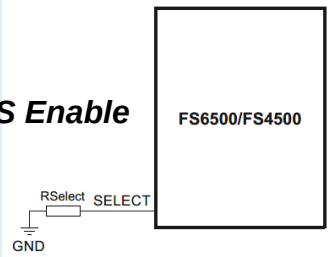
LPOFF Mode (all Regulators shut down, RSTB/FS0B/FS1B/INTB =0)

- *LPOFF-Sleep mode can enter by SPI command(GO_LPOFF bit =1 in MODE Register) and device can enter LPOFF-Sleep mode only when device is in Normal Mode;*
- *LPOFF_AUTO_WU can enter by SPI Command(LPOFF_AUTO_WU bit =1 in MODE Register) or VPRE<VPRE_UV_L4P3(both INIT and Normal Mode).*
- *Device can be wake up by CAN/LIN/IO/LDT when in LPOFF-Sleep Mode.*
- *Fail safe registers configuration will lost to default value after wake up from LPOFF mode;*
- *Main registers configuration will not lost after wake up from LPOFF mode;*

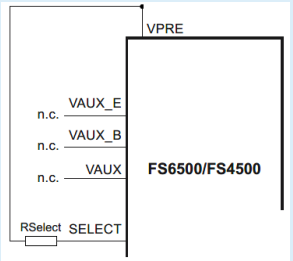
Deep Fail safe Mode(DFS, all Regulators shut down, RSTB/FS0B/FS1B/INTB =0)

- *DFS Enable and Disable*

DFS Enable



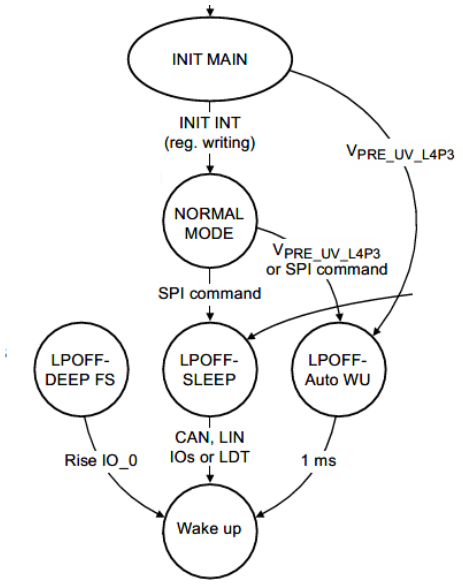
DFS Disable



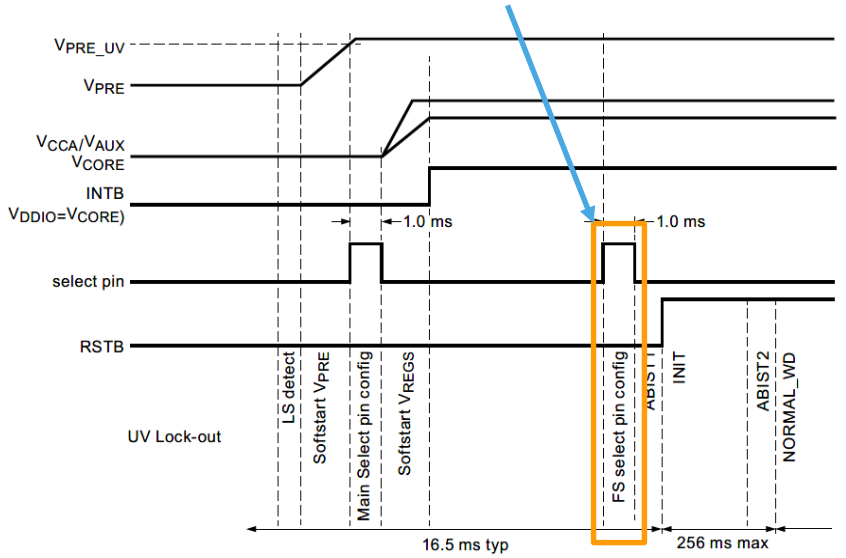
- *DFS Enable/Disable is detected in **FS Select pin Config** phase and will not change if hardware connection change after FS Select pin Config phase.*
- *Fail safe registers configuration will lost to default value after wake up from DFS mode;*
- *Main registers configuration will not lost after wake up from DFS mode;*
- ***DFS wake up only through IO0 go to low level(<2.1V) first, then go to high level(>2.6V);***

DFS mode entry and behavior when DFS enabled/disabled:

Configuration	***Fault Error Counter = Max Value***	***RSTB low sustain >8s***
DFS Enable	*Enter DFS*	*Enter DFS*
DFS Disable	*NO Enter DFS*	*Enter LPOFF*



DFS configuration detected



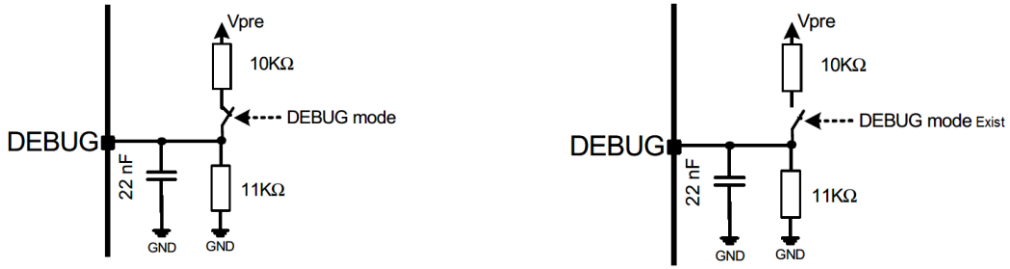
DEBUG MODE: HOW TO ENTER/EXIST DEBUG MODE? WHAT IS SPECIAL FOR DEBUG MODE

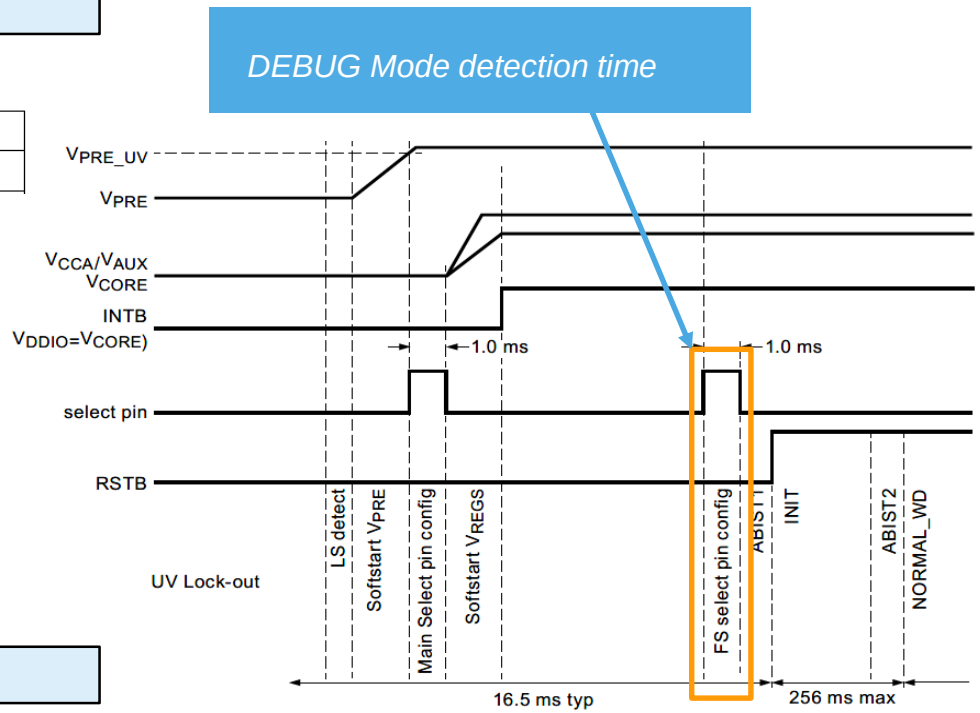
How to enter DEBUG Mode?

- *Debug pin voltage should be between 2.8V to 4.35V when device Power up.*

V_{DEBUG_IL}	Low input voltage threshold	2.1	2.35	2.8	V	
V_{DEBUG_IH}	High input voltage threshold	4.35	4.6	4.97	V	

- *Debug mode is detected at FS select pin config phase, if debug pin voltage change after this phase, will not impact debug mode entry/exist.*
- *Recommended hardware connection*





How to exist DEBUG Mode?

- *Leave Debug pin voltage <2.1V and Power up again.*

What's special in DEBUG Mode?

1. ***Watchdog work in debug mode:*** *watchdog can refresh any time and no watchdog window limitation.*

Mode	NO watchdog refresh (timeout)	Right watchdog refresh	Wrong watchdog refresh
Debug	*no impaction*	*no impaction*	*Action same as non-debug mode*

2. ***DFS is disabled***

   fault error counter reach max value → do not enter DFS.

   RSTB asserted low >8s → do not enter DFS or LPOFF.

FS45/FS65 SAFETY FUNCTIONS

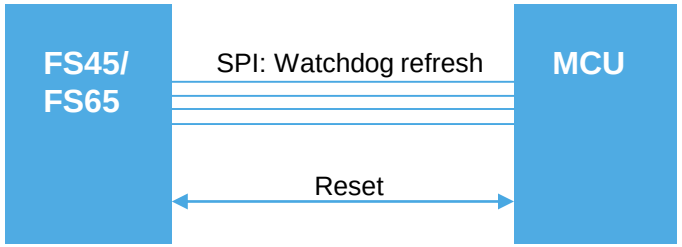
QUESTIONS

- ***Watchdog:*** *What's Watchdog Content requirement? What's Watchdog refresh Time requirement ?*
- ***Watchdog:*** *What's the watchdog errors in INIT_FS/NORMAL_WD Phase?*
- ***Watchdog:*** *How watchdog error counter works?*
- ***Watchdog:*** *How to Disable Periodic Watchdog ? How to change Watchdog Window time at Normal_WD phase?*
- ***RESET:*** *What's reset Trigger Source and how to Configure Trigger Source ?*
- ***FS0B/FS1B:*** *How to release FS0B/FS1B, check list when FS0B/FS1B cannot release ?*
- ***FS1B:*** *How to configure FS1B delay time ? What's the behavior when device enter DFS/LPOFF/POR?*
- ***Fault error Counter:*** *How to increase/ decrease fault error counter value?*
- ***ABIST1/ABIST2:*** *What's the Check items?*
- *How to do code update with CAN in the garage ?*
- *FS45,FS65 ASILB & FS45,FS65 ASIL D Compliant ?*

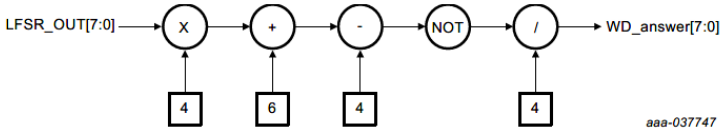
WATCHDOG: WHAT'S WATCHDOG CONTENT REQUIREMENT? WHAT'S WATCHDOG REFRESH TIME REQUIREMENT ?

- *Watchdog refresh is conducted through SPI between MCU and FS45/FS65.*
- *FS45/FS65**(ASIL D)** integrated challenger watchdog mechanism, it requires right **watchdog content** and right **watchdog refresh time**.*

What's Watchdog Content requirement(ASIL D)?



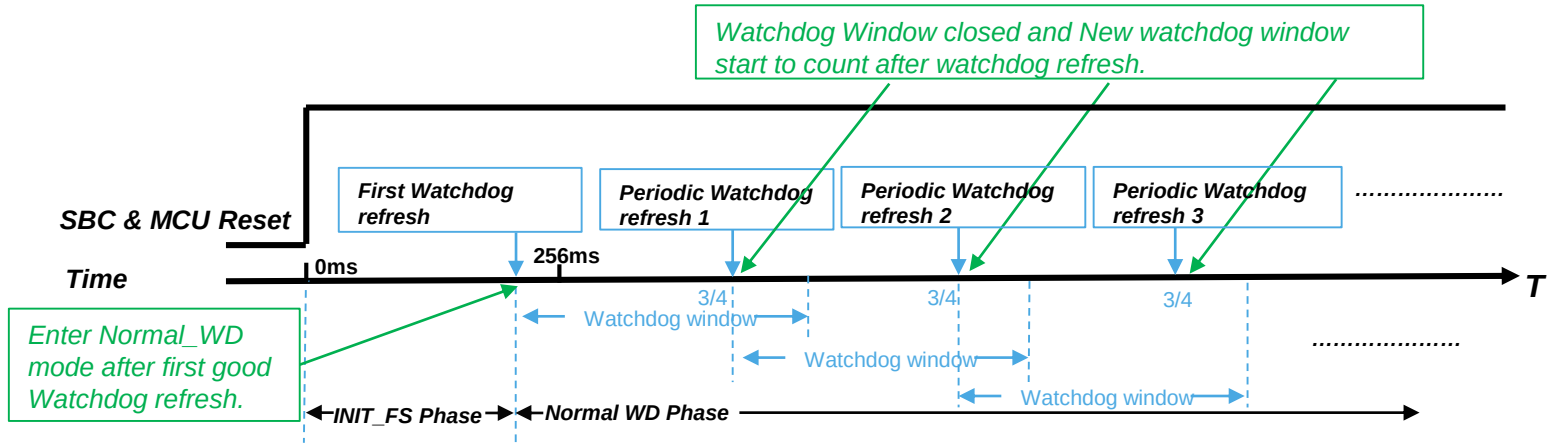
1. *MCU read FS45/FS65 WD_LFSR Register to get LFSR value.*
2. *MCU Compute Answer based on below formula.*



3. *MCU Write the answer to FS45/FS65 WD_ANSWER register.*
4. *For example, LFSR is 0xB2, WD_ANSWER is 0x4D.*

Note: LFSR value changed every time WD_ANSWER register is written or watchdog timeout.

What's Watchdog refresh Time requirement ?

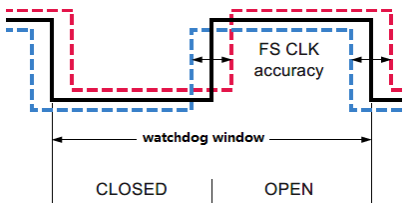


INIT_FS Phase:

1. *First watchdog must refresh within 256ms after Reset release to high & all fail safe INIT Registers configuration are finished.*
2. *If first watchdog refresh correctly during 256ms, FS65 enter Normal_WD phase directly(do not wait for 256ms counter end). Periodical watchdog refresh is needed and watchdog error/refresh counter start to work in Normal_WD Phase.*

Normal_WD Phase:

1. *After First watchdog refresh finished, MCU must refresh watchdog periodical, Periodical watchdog window has close window and Open window. watchdog must be refreshed at open window and **highly recommended to Periodical refresh at 3/4 of watchdog window as FS CLK accuracy is 10%.***
2. *New watchdog window counter starts at the time wrong watchdog refresh or good watchdog refresh or watchdog window timeout.*



		Window	
		CLOSED	OPEN
SPI	BAD key	WD_NOK	WD_NOK
	GOOD key	WD_NOK	WD_OK
	None (timeout)	No_issue	WD_NOK

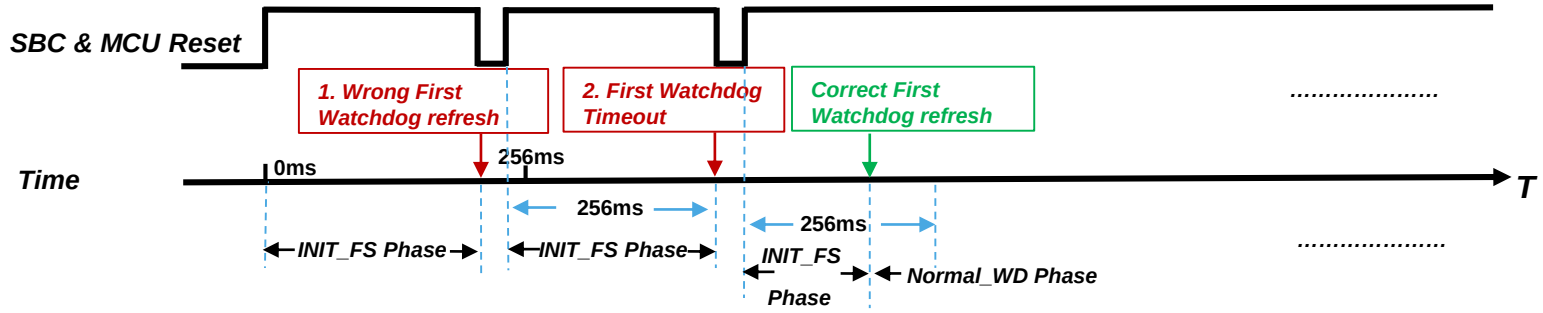
WATCHDOG: WHAT'S THE WATCHDOG ERRORS IN INIT_FS/NORMAL_WD PHASE?

What's the watchdog errors in INIT_FS Phase ?

Watchdog errors at INIT_FS Phase: there are 2 kinds of watchdog errors at INIT_FS phase, Reset will asserted to low when errors happen.

Error 1: *If first watchdog refresh not Correct, FS45/FS65 Reset directly, FS45/FS65 enter INIT_FS mode again and request first correct watchdog refresh within 256ms.*

Error 2: *If first watchdog did not refresh within 256ms, FS45/FS65 Reset directly, FS45/FS65 enter INIT_FS mode again and request first correct watchdog refresh within 256ms.*



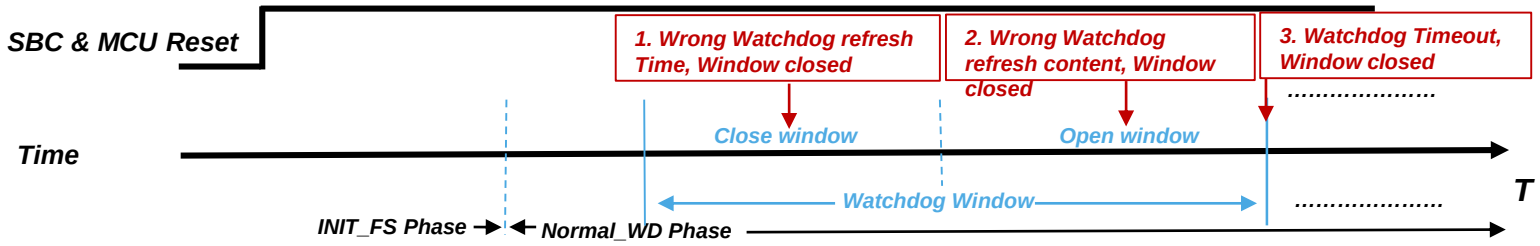
What's the watchdog errors in Normal_WD Phase ?

Watchdog Errors at Normal WD Phase: there are 3 kinds of watchdog errors at Normal_WD phase.

Error1: *watchdog refresh at close window. WD_BAD_TIMING =1 in WD_ANSWER register.*

Error2: *watchdog refresh at open window but watchdog answer is wrong; WD_BAD_DATA =1 in WD_ANSWER register.*

Error3: *watchdog did not refresh at whole watchdog window, watchdog timeout. WD_BAD_TIMING =1 in WD_ANSWER register.*



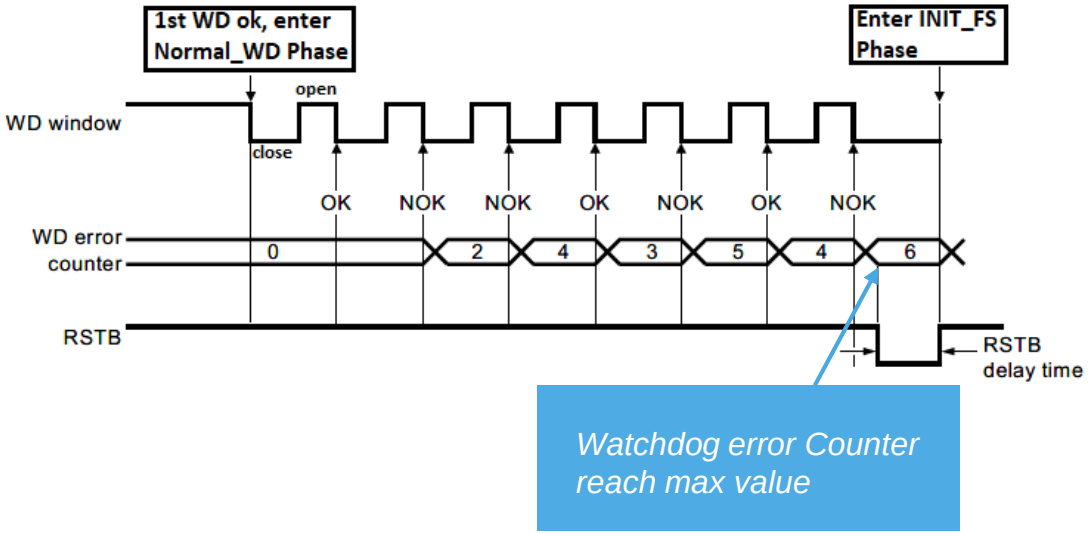
Note: In NORMAL_WD mode, one watchdog error did not cause RSTB/FS0B Asserted to low , When WD error Counter reach max value, RSTB&FS0B react can be configured by WD_IMPACT_1:0 bits.

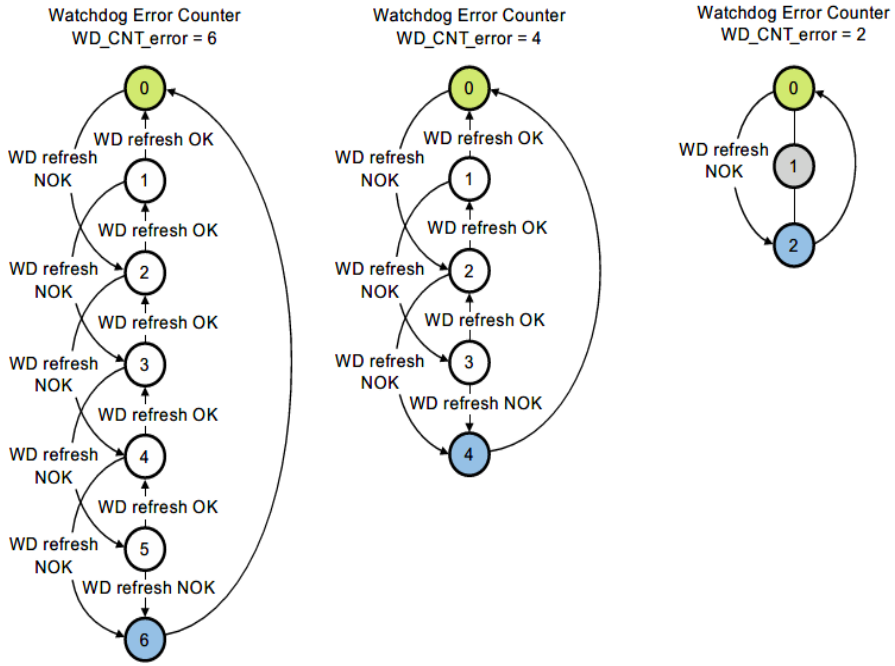
WATCHDOG: HOW WATCHDOG ERROR COUNTER WORKS?

How watchdog error Counter works?

Watchdog error counter: ***work in Normal_WD phase****. Max value[2 or 4 or 6(default)] is configured in WD_CNT_ERR_1:0 bits, INIT_WD_CNT register.*

- *Wrong watchdog: Counter +2; right watchdog: Counter-1,*
- *When Watchdog error Counter reach max value, safety action by default : 1. fault error counter +1; 2. RSTB asserted to Low;*
- *Watchdog error counter max value can impact NONE/RSTB/FS0B/RSTB&FS0B, it is configured by WD_IMPACT_1:0 bits in INIT_SF_IMPACT Register.*





Watchdog error counter count rules

- *If WD_IMPACT_1:0 = 01 configured to impact RSTB when watchdog error Counter reach max value,*

FS65 will enter INIT_FS mode after RSTB released to high.

- *If WD_IMPACT_1:0 = 00/10 did not impact RSTB, FS65 will still at Normal_WD phase when*

Watchdog error counter reach max value.

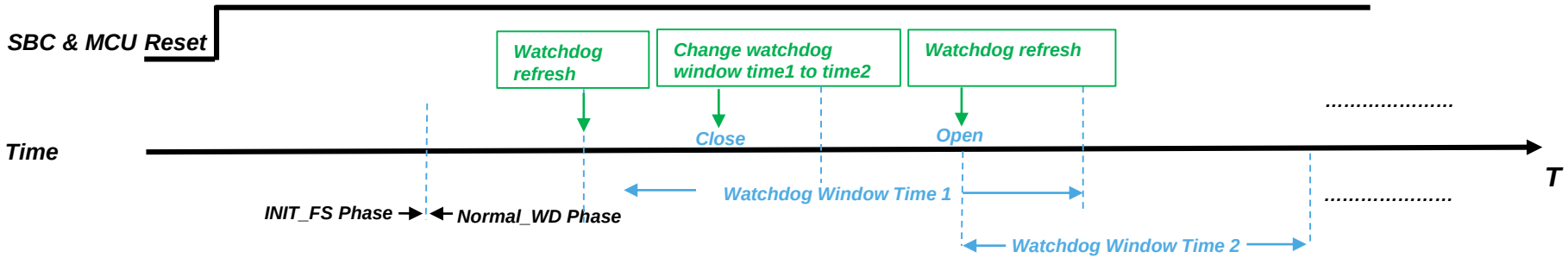
- ***If WD_IMPACT_1:0 = 00 did not impact RSTB or FS0B, fault error counter will not increase, when watchdog error counter reach max value.***

WATCHDOG: HOW TO DISABLE PERIODIC WATCHDOG ? HOW TO CHANGE WATCHDOG WINDOW TIME AT NORMAL_WD PHASE ?

How to Disable Periodic Watchdog ?

- *Periodic watchdog can be disabled by configuring WD_WINDOW_3:0 = 0000 in WD_WINDOW Register* ***(only can be configured in INIT_FS phase)***
- ***First watchdog refresh in INIT_FS phase(within 256ms) is needed and period watchdog refresh is not needed when watchdog window is 0.***
- ***When watchdog window is 0, watchdog can be refreshed without time limitation(except first watchdog refresh). Fault error counter will be decreased when watchdog refresh counter reach max value.***
- ***When watchdog window is 0, bad watchdog refresh will increase watchdog error Counter and increase fault error counter when watchdog error counter reach max value.***

How to change Watchdog Window time at Normal_WD phase ?



1. *When in Normal_WD Phase, change watchdog window in WD_WINDOW register at close window.(cannot change to 0ms in Normal_WD)*
2. *Watchdog refresh according to the watchdog window time before change in open window.*
3. *After watchdog refresh, new watchdog window will be valid, need to refresh watchdog according to new watchdog time window.*
4. ***If watchdog refresh is not correct or watchdog time out, new watchdog window time will also be valid in the coming window.***

RESET: WHAT'S RESET TRIGGER SOURCES AND HOW TO CONFIGURE TRIGGER SOURCE?

How to configure RSTB activation or non-activation for the faults?

The activation of RSTB depends on the fail-safe state machine configuration performed during the INIT_FS phase.

The following faults impact on RSTB activation can be configured:

- Watchdog error counter = max value (6 by default) → *INIT_SF_IMPACT Register: WD_IMPACT_1:0*
- VCORE, VCCA, VAUX undervoltage → *INIT_VCORE_OVUV_IMPACT/ INIT_VCCA_OVUV_IMPACT/ INIT_VAUX_OVUV_IMPACT Register*
- VCORE, VCCA, VAUX overvoltage → *INIT_VCORE_OVUV_IMPACT/ INIT_VCCA_OVUV_IMPACT/ INIT_VAUX_OVUV_IMPACT Register*
- FCRBM follows VCORE configuration → *INIT_VCORE_OVUV_IMPACT Register, same configuration with Vcore*
- IO_23 error detection (FCCU) → *INIT_FSSM Register: IO_23_FS bit*
- Fault error counter level → *INIT_FAULT Register: FLT_ERR_IMP_1:0 bits*

The following faults impact on RSTB activation cannot be configured:

- VPRE overvoltage
- Watchdog refresh not OK or watchdog timeout during INIT phase
- FS0B short to high
- RSTB pulse requested by SPI

How to check RSTB Source when RSTB happen ?

1. Check RSTB low duration.

- *If RSTB low duration is not close to configured RSTB low duration INIT_FSSM RSTB_DURATION bit, it is most probability External Reset. Reading DIAG_SF_IOs register RSTB_EXT bit to confirm whether it is an external REST.*
- *If RSTB low duration is close to configured RSTB low duration, it is most probability caused by SBC.*

2. Check if the Reset happen once or frequently

- *If once, please check regulators output when RSTB low with oscilloscope, please also check if there is OV/UV flag reported.*
- *If Reset happen frequently, Please check if the time cycle is related to watchdog and watchdog error counter max value.*

3. Check when RSTB Happen

- *If RSTB asserted to low as soon as first right watchdog refresh, it is mostly caused by FCCU error, please check DIAG_SF_IOs register, IO_23_FAIL bit.*
- *FCCU Error can be confirmed by configuring INIT_FSSM: IO_23_FS bit =0 to see if the failure removed.*

FS0B/FS1B: HOW TO RELEASE FS0B/FS1B, CHECK LIST WHEN FS0B/FS1B CANNOT RELEASE

How to release FS0B/FS1B ?

- ***First, SPI Read BIST Register : LBIST_OK& ABIST1_OK must be "1", otherwise, FS0B/FS1B cannot be released.***
- ABIST2_FS1B_OK=1 if part number with FS1B → ***SPI Write BIST Register: ABIST2_FS1B=1***
- ABIST2_VAUX_OK=1 except if VAUX_FS_OV_1:0=VAUX_FS_UV_1:0="00" → ***SPI Write BIST Register, ABIST2_VAUX=1***
- Fault is removed
- Fault error counter must be at '0' → ***7* successful continuous watchdog refresh can clear Fault error counter from 1 to 0***
- Close the S1 switch if FS1B backup delay was engaged (FS1B_DLY_DRV bit = 1) → ***SPI Write SF_OUTPUT_REQUEST register: FS1B_DLY_REQ =0***
- RELEASE_FSxB register must be filled with the right value

1. ***Read Latest LFSR value(WD_LFSR register).***
2. ***Calculate release command based on Rules in the right.***
3. ***SPI write release command to RELEASE_FSxB register.***

	WD_LFSR_7:0	b7	b6	b5	b4	b3	b2	b1	b0
Release FS0B	RELEASE_FSxB_7:0	0	1	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b3}$	$\overline{b4}$
Release FS1B	RELEASE_FSxB_7:0	1	1	0	$\overline{b3}$	$\overline{b4}$	$\overline{b5}$	$\overline{b6}$	$\overline{b7}$
Release FS0B and FS1B	RELEASE_FSxB_7:0	1	0	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b6}$	$\overline{b7}$

What's the Check List when FS0B/FS1B cannot be released ?

1. ***Check LBIST ABIST1, ABIST2 result in BIST register***

   If LBIST fail, there is something wrong in the Chip.

   If ABIST1 fail, please check if Vpre, Vcore, Vcca, Vaux regulators output stable before RSTB release to high.

2. ***Check fault error counter value by reading DIAG_FS_ERR register, FLT_ERR_2:0 bits***

   If fault error counter value is not 0, please check if FCCU report error by reading IO_23_FAIL bit.

   Please check if there is watchdog error by reading WD_BAD_TIMING/WD_BAD_DATA bits.

   Please check if other faults, like UV/OV;

3. ***Check release command and release time***

   Release command should align with the rules.

   The RELEASE_FSxB write command must be done after the WD_LFSR read command, within the same WD period.

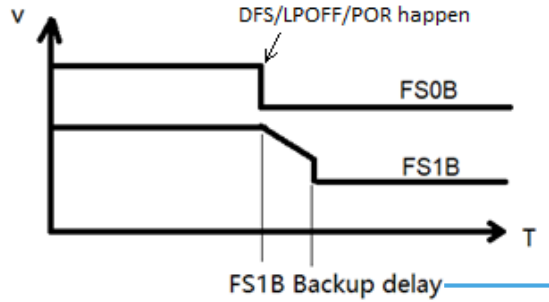
FS1B: HOW TO CONFIGURE FS1B DELAY TIME ? WHAT'S THE BEHAVIOR WHEN DEVICE ENTER DFS/LPOFF/POR?

How to configure FS1B delay time ?

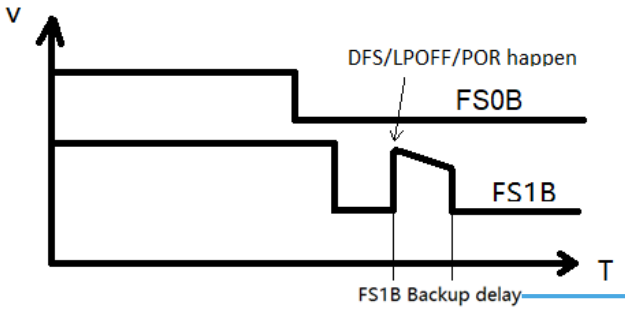
- *FS1B delay mode can be configured in software by writing INIT_SF_IMPACT register, TDLY_TDUR =0.*
- *FS1B delay time can be configured in INIT_FS1B_TIMING register, FS1B_TIME_3:0 bits and INIT_SUPERVISOR register: FS1B_TIME_RANGE bit, longest delay time is 3.15s.*
- *FS1B Back up delay is determined by External Rpd and Cpd in Vpu_fs pin. When Switch S1 open, Cpd discharge through Rpd, FS1B will be asserted to low when Vpu_fs voltage decreased to 3.2V from ~5.4V. Switch S1 is controlled by FS1B_DLY_REQ bit(open by default) in SF_OUTPUT_REQUEST register.*

What's FS1B behavior when device enter DFS/LPOFF/POR?

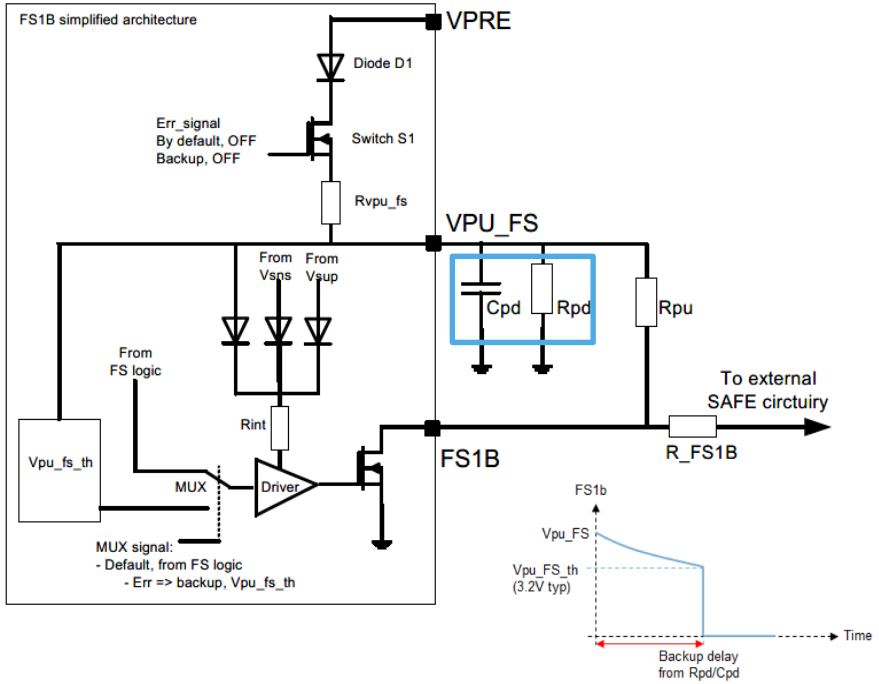
(1) FS1B is high before enter DFS/LPOFF/Power Down.



(2) FS1B is low before enter DFS/LPOFF/Power Down.



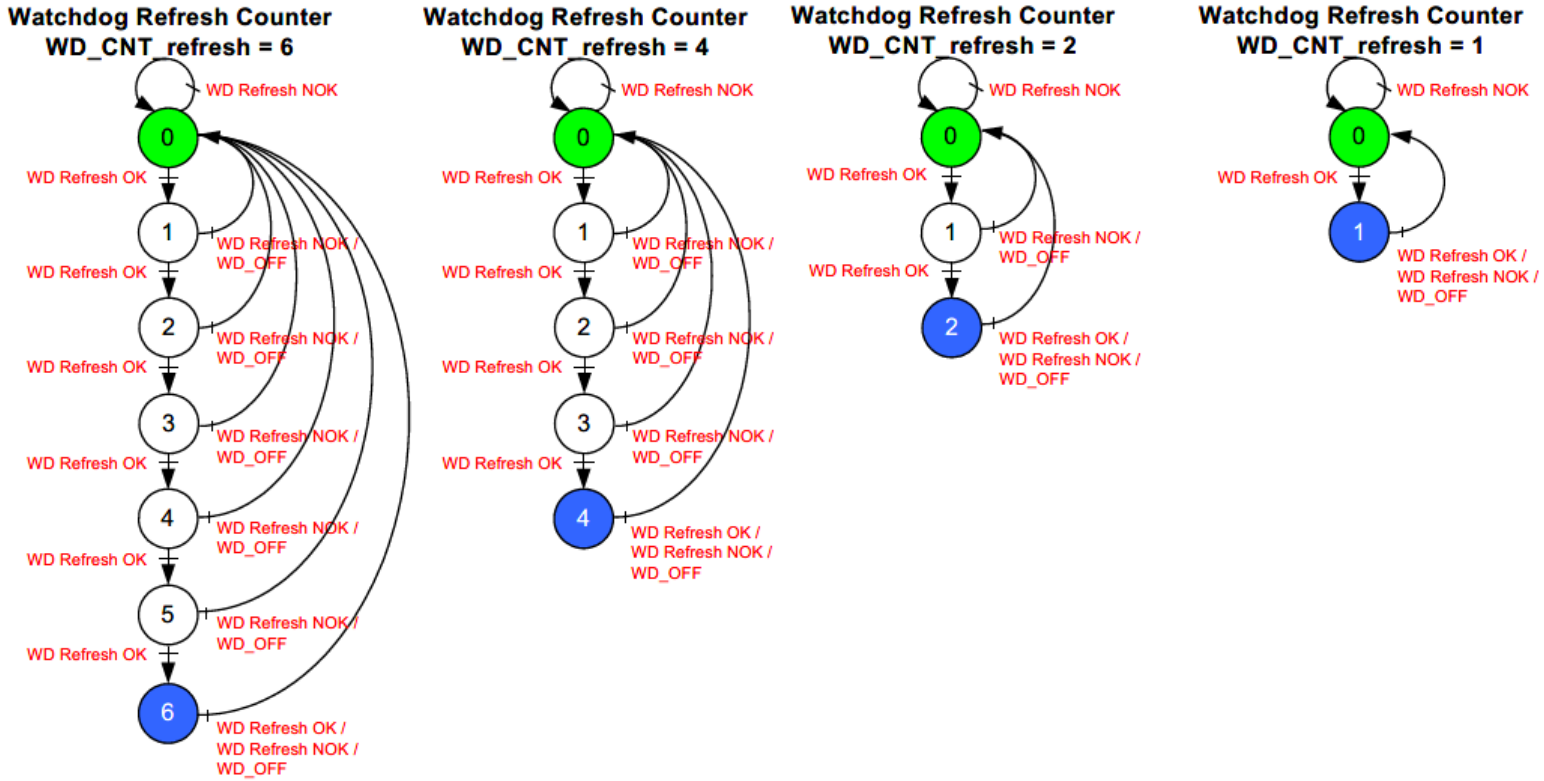
The FS1B backup delay time is determined by Cpd and Rpd, If this FS1B backup delay is not expected, Please remove Cpd and Rpd(shown in The picture in the right side).



FAULT ERROR COUNTER: HOW TO INCREASE/ DECREASE FAULT ERROR COUNTER VALUE?

How to increase/ decrease fault error counter value?

- *Fault error Counter value reach max value, device enter DFS mode, all regulators shut down. Max value can be 2,4,6(default) by SPI Writing INIT_FAULT Register, FLT_ERR_FS bit.*
- ***Fault error counter increase:** fault error counter is 1 by default when powerup or wakeup from LPOFF, fault error counter increase every time RSTB,FS0B asserted to low.*
- ***Fault error Counter decrease:** Fault error Counter value decrease when watchdog refresh counter reach max value. Watchdog error counter max value can be configured to 2,4,6(default) by writing INIT_WD_CNT Register: WD_CNT_RFR_1:0 bits.*



ABIST1/ABIST2:WHAT'S THE CHECK ITEMS

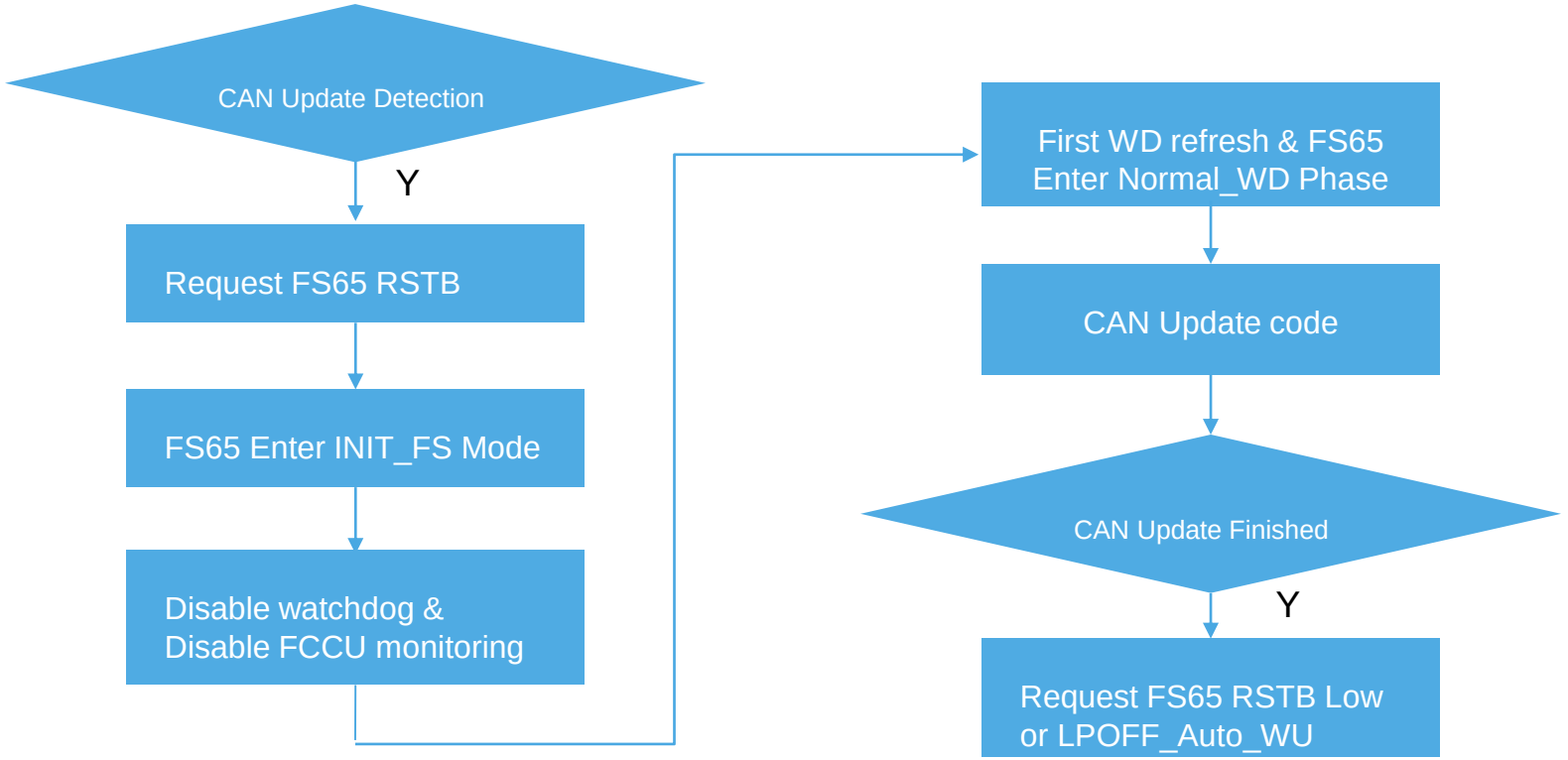
	ABIST1 automatic			ABIST2 on demand			Comment
	OV	UV	OK/NOK	OV	UV	OK/NOK	
Vpre	x						UV from cascaded regulators (Vcore, Vcca, Vaux)
Vcore	x	x					Both UV/OV checked
Vcca	x	x					Both UV/OV checked
Vaux				x	x		Both UV/OV checked
V2p5 Main Digital	x						UV means power on reset state
V2p5 Main Analog	x						UV means power on reset state
V2p Fail-Safe Digital	x						UV means power on reset state
V2p Fail-Safe Analog	x						UV means power on reset state
Osc Fail-Safe			x				+/-50% clock deviation
RSTb			x				- Short to High detected during ABIST
							- Short to GND detected when RSTb is released by PowerSBC (safe state by default)
							- Open detected when RSTb is released by PowerSBC (safe state by default)
FS0b			x				- Short to High detected during ABIST (RSTb released)
							- Short to GND detected when FS0b is released by PowerSBC (safe state by default)
							- Open detected when FS0b is released by PowerSBC (safe state by default)
FS1b						x	- Short to High detected during ABIST (RSTb released)
							- Short to GND detected when FS1b is released by PowerSBC (safe state by default)
							- Open detected when FS1b is released by PowerSBC (safe state by default)

- Vaux and FS1b ABIST are done on demand. FS0b remains asserted low until ABIST is executed and PASS.
- ABIST result is reported by 3 SPI bits (ABIST_startup, ABIST_Vaux, ABIST_FS1b)
- LBIST OK is also reported by SPI

2.13 In-vehicle programming

For in-vehicle programming at the garage, if the debug mode cannot be used, the watchdog refresh can be disabled during INIT_FS state of the fail-safe logic to allow programming without taking care of the watchdog refresh. INIT_FS can be entered by a reset request with RSTB_REQ bit in SF_OUTPUT_REQUEST register. It is also recommended to disable the FCCU monitoring to avoid unexpected FCCU error detection during the programming by setting IO_23_FS bit at '0' in INIT_FSSM register. The watchdog disable is effective when the INIT_FS is closed and requires at least one good watchdog refresh within the 256 ms of the INIT_FS timeout.

When the programming is complete, reset the MCU by a reset request with RSTB_REQ bit in SF_OUTPUT_REQUEST register to execute the new software and enable the watchdog again or send the device to LPOFF_Auto_WU to restart the MCU from a power on reset and execute the new software.



FS45,FS65 ASILB & FS45,FS65 ASIL D COMPLIANT

Different Items	FS45, FS65 (ASILB)	FS45, FS65 (ASIL D)
LIN only, No CAN FD Part	*Yes*	*No*
Functional Safety	*No LBIST*	*LBIST*
	NO FCCU	*FCCU*
	Simple Watchdog	*Challenger watchdog*

FS45XX/FS65XX(ASIL B) and FS45XX/FS65XX(ASIL D) are hardware and software compatible when customer change system target from ASIL D to ASIL B.

- ***Hardware: FS45/FS65(ASIL B) can replace FS45/FS65(ASIL D) without Changing hardware when they have same current capability and same functions.***
  For example: FS6507CAE can replace FS6502CAE without hardware change.
- ***ASIL B**: IO2,IO3 are no wakeup capability by default; no FCCU monitoring, so regardless of IO2,IO3 connection. **ASIL D**: IO2,IO3 are FCCU by default.*
- ***Software: ASIL D version driver can be used by ASILB version, no need change when they have same functions.***
- *LBIST_OK bit in ASIL B Version is "Reserved =1";*
- *ASIL B: IO2,IO3 are no FCCU monitoring function in Version, regardless of hardware connection and no error report.*
- *ASIL B: Simple watchdog regardless of watchdog content, any content is OK, just watchdog time is required same as ASILD Version.*

***Note:** FS45xx/FS65xx(ASIL B) has LIN only(No CAN FD) parts, like FS45xxK, FS65xxK, Pin8, Pin9, Pin20, Pin21 must be left open. While, FS45xx/FS65xx(ASIL D) parts are LIN & CAN FD together.*

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